DESIGN, FABRICATION AND STUDY OF D.C. CHARACTERSTICS OF HIGH FREQUENCY TRANSISTORS

A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of
MASTER OF TECHNOLOGY

By
RAVENDER GOYAL

to the

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY KANPUR
AUGUST, 1978

CERTIFICATE

It is certified that the work entitled "Design, Fabrication and Study of D.C. Characteristics of High Frequency Transistors", by Ravender Goyal has been carried out under my supervision and it has not been submitted elsewhere for a degree.

M. S. Tyagi

M.S. Tyagi
Professor
Electrical Engg. Department
Indian Institute of Technology
Kanpur(India)

Date: Aug.7, 1978

EE-1978-M-GOY-DES

ACKNOWLEDGEMENT

I have a pleasure in expressing my deep sense of gratitude to Dr. M.S. Tyagi for having suggested this problem to me. His constant guidance and encouragement throughout the work is beyond mention. Association with Dr. Tyagi has considerably enhanced my understanding of semiconductor devices.

I thank Mr. R.S. Korde for his help in the mask design and sharing his experience with me during the device fabrication. Fruitful discussions with Mr. G.V. Ram are also acknowledged.

I wish to thank Mr. K.D. Dwivedi for assisting me during some measurements.

I take this opportunity to remember to myself, my colleagues P.N. Goswami and Davendra Shankar who spent countless memorable sessions with me.

A lot is left unsaid for my parents whose constant encouragement has made this work possible in the present state.

Ravender Goyal

ABSTRACT

High frequency transistors with three different emitter geometries have been designed and fabricated in the laboratory with available facilities.

Base diffusion was performed using BN wafer source and the standard pre-deposition and drive-in cycle. Arsenic has been used as a dopant to obtain nearly box-type distribution in the emitter. The use of arsenic results in a shallow, uniform emitter-base junction and minimizes the "emitter-dip" effect.

The fabricated devices have a base-width of .3 μm. The minimum horizontal dimensions down to 7.5 μm could be successfully realised with a resolution of 2.5 μm, using photolighography.

The doping profiles in the base and the emitter regions have been determined experimentally.

The common-emitter current gain of the device has been calculated from the knowledge of the material and device parameters. The effects of bandgap narrowing, carrier impurity scattering and the S-R-H (Shockley-Read-Hall) recombination, together with the effect of heavy doping on Einstein's relation have been taken into account in the calculation of the current gain. A comparison between the computed and the measured results is made and the discrepancy between the two is explained. The variation of current gain with injection level is studied. It is observed that the

initial rise in the current gain is due to the dominance of injection current over the surface leakage current and the sharp fall at high injection level is mainly due to emitter crowding.

The dependence of maximum value of the current gain and the current-carrying capability of the device on emitter-geometry has also been investigated.

TABLE OF CONTENTS

	Page
List of Symbols	viii
List of Figures	xi
List of Tables	xii
CHAPTER	
1 INTRODUCTION	1
1.1 State-of-the-Art	2
1.2 Objectives of the Present Work	3
2 DESIGN CONSIDERATIONS	6
2.1 Design Constraints	7
2.1.1 Gain Band-Width Frequency	8
2.1.2 Calculation of Parasitic Elements	11
2.2 Design of High Frequency Transistors	13
2.2.1 Horizontal Geometry	14
2.2.2 Choice of the Substrate	14
2.2.3 Vertical Geometry	15
2.3 Ohmic Contacts	16
3 FABRICATION TECHNOLOGY	19
3.1 Starting Material	20
3.2 Oxidation	20
3.3 Photoengraving	21
3.3.1 Surface Preparation	21
3.3.2 Photoresist Coating	22
3.3.3 Pattern Delineation in Photoresist	22
3.3.4 Oxide Delineation	23
3.4 Base Diffusion	24
3.4.1 BN Wafer Surface Activation and Stabilization	24

CHAPTER

		Page
	3.4.2 Predeposition	25
	3.4.3 Drive-in-Diffusion	26
	3.5 Emitter Diffusion	27
	3.6 Back Surface Preparation	28
	3.7 Contact Opening	29
	3.8 Metallization and Contact Etching	29
	3.8.1 Metallization	29
	3.8.2 Metal Etching	30
4	DETERMINATION OF DOPING PROFILES AND MEASUREMENT OF D.C. PARAMETERS	34
	4.1 Measurement of Junction Depths	34
	4.2 Evaluation of Doping Profiles	35
	4.2.1 Emitter Profile	35
	4.2.2 Base Profile	36
	4.3 Junction I-V Characteristics	37
	4.4 Set of V_{CE}-I_C Curves of a Typical Transistor	38
	4.5 Measurement of I_B and I_E as a Function of V_{EB}	38
	4.6 Measurement of $h_{FE_{max}}$ and the Current-Carrying Capability of the Transistors	40
5	RESULTS AND DISCUSSION	48
	5.1 Calculation of Common-Emitter Current Gain	48
	5.2 Factors Which Degrade the Common-Emitter Current Gain	53
	5.3 Variation of h_{FE} with Injection Level	55
	5.4 Dependence of Maximum Current-Gain and Current-Carrying Capability on the Horizontal Geometry	57
6	CONCLUSION	61
	APPENDIX	63
	REFERENCES	65

List of Symbols

A_E	emitter area.
C_{CI}	collector capacitance under emitter region.
C_{CO}	collector capacitance outside emitter region.
C_{TE}	emitter-base junction capacitance.
C_{TC}	transition capacitance of the base-collector junction.
D	diffusion constant.
D_{pE}	diffusion constant of holes in emitter.
D_{nB}	diffusion constant of electrons in base.
$\bar{D}_{pE}, \bar{D}_{nB}$	effective values of D_{pE}, D_{nB}.
f_T	gain band-width frequency.
h_{FE}	common-emitter current gain.
$h_{FE_{max.}}$	maximum value of h_{FE}
I_B, J_B	base current, base current density.
I_E	emitter current.
I_C, J_C	collector current, collector current density.
J_I	injection current density.
l	emitter length
L_s	collector substrate thickness not covered by the base-collector junction depletion-region.
L_{pE}	diffusion length of holes in emitter.
L_{nB}	diffusion length of electrons in base.
m	phase factor.
n	drift field factor.

$n_e(0)$	excess minority-carrier concentration in base.
N_E, N_B, N_C	maximum doping concentration in emitter, base, collector.
$\bar{N}_E$, $\bar{N}_B$	effective majority carrier concentration in emitter, base.
N_{BE}	base doping concentration at emitter-base junction vicinity.
N_{BC}	base doping concentration at base-collector junction vicinity.
$\bar{Q}_E, \bar{Q}_B$	effective value of Gummel Number in emitter, base.
r'_c	resistance of collector region.
r_e	emitter-base junction resistance.
r'_b	base-spreading resistance.
r'_{b1}, r'_{b2}	components of r'_b.
R_c	base contact-resistance.
S_1, S_2, S_3	refer to Fig.2.3.
V_{SL}	scattering limited velocity of carriers.
V_{BC}	base-collector junction reverse-bias voltage.
V_{EB}	emitter-base junction forward-bias voltage.
V_{CE}	collector to emitter voltage.
W_B	base-width.
W, W_1, W_2	components of base-width (Fig.2.3).
X_{JE}, X_{JC}	emitter-base, base-collector junction depth.
X_{de}, X_{db}	emitter-base, base-collector junction depletion-layer width.
k	Boltzmann Constant.
K	arbitrary constant.

q	electronic charge.
T	absolute temperature.
τ_{ec}	total time delay.
τ_b	base transit time.
τ_c	collector R-C charging time.
τ_d	collector depletion-layer transit time.
τ_e	emitter-base junction time-constant.
τ_{nB}	life time of electrons in base.
τ_{pE}	life time of holes in emitter.
ρ_1	average resistivity of the base region under the shadow of emitter area.
ρ_2	average resistivity of the base region between emitter-edge and the base contact.
ρ_c	collector substrate resistivity.
$\rho_s(x)$	sheet resistance at some distance x.
ε_s	material dielectric constant.
η	ideality factor.
φ	junction built-in voltage.
α	Caughey-Thomas parameter.
β	doping profile parameter.

List of Figures

Fig.No.	Caption	Page
2.1	Typical High Frequency Transistor Horizontal Geometries.	17
2.2	One-Dimension View of a Junction Transistor.	18
2.3	Cross-section of a Planar Bipolar Transistor.	18
3.1	Typical Horizontal Geometry of the Three Transistors Fabricated.	32
3.2	Photograph (1x100) of a Typical Set of Fabricated Transistors with Three Different Emitter Geometries.	33
4.1	Plot of Typical Doping Profile in Various Regions of the Transistor.	42
4.2	Emitter-Base Junction I-V Characteristics of a Typical Transistor.	43
4.3	Base-Collector Junction I-V Characteristics of a Typical Transistor.	43
4.4	Set of V_{CE}-I_C Curves for a Typical Transistor (Geometry (1)).	44
4.5	Circuit Arrangement for the Measurement of I_B and I_E as a Function of V_{EB}.	44
4.6	Plots of I_C and I_B vs V_{BE} and h_{FE} vs I_E for a Typical Transistor Geometry (1)	45
4.7	Plots of I_C and I_B vs V_{BE} and h_{FE} vs I_E for a Typical Transistor Geometry (2)	46
4.8	Plots of I_C and I_B vs. V_{BE} and h_{FE} vs. I_E for a Typical Transistor Geometry (3).	47

List of Tables

Table No.		Page
1.1	Present State-of-the-Art of High Frequency Bipolar Transistors	5
4.1	$h_{FE_{max.}}$ and Current-Carrying Capability Measurements	41
5.1	Profile and Structural Parameters of the Transistor Used in Calculations	59
5.2	Caughey-Thomas Parameters	59
5.3	Minority Carrier Lifetimes and Computed Values of Effective Diffusion Constants and Diffusion Lengths	60
5.4	Computed Values of Bandgap Narrowing, Effective Gummel Number and Effective Majority-Carrier Concentrations	60

CHAPTER 1

INTRODUCTION

In recent years, the phenomenal development in the field of communication engineering has led the trend to go for higher and higher frequencies. This has resulted in larger bandwidth requirement in most of the modern communication system. These systems require cheap and reliable devices with high power gain, low noise and high power output in the higher frequency region. A number of devices capable of operating at these high frequencies are GaAs FET, TRAPATT, IMPATT and bulk GaAs devices along with conventional bipolar transistors.

Inspite of the fact that FETs are coming up rather fast, much efforts have gone to increase the power output and operating frequency of bipolar transistors. One of the main parameters which controls the maximum frequency of operation $f_{max.}$ is the choice of high carrier mobility material. As the low-field mobility of electrons in GaAs is more than double of that in silicon, GaAs devices promise better high frequency performance over silicon devices. However, silicon is still preferred over GaAs for high frequency bipolar transistor fabrication because of a number of reasons such as advance state of silicon technology, ease of fabrication, higher efficiency, reproducibility and low cost.

A bipolar transistor which is capable of operating at high frequencies in the range of several hundred MHz is classified as high frequency transistor. The main difference between high frequency and low frequency bipolar transistors lies in their physical dimensions, which are greatly reduced as the operating freq increases. The critical parameters governing the value of f_{max}, may be summarised as follows:

-- base-width

-- collector doping concentration

-- doping-profiles in the emitter and the base regions.

-- parasitic resistances and capacitances.

1.1 State-of-the-Art

Till 1960, bipolar transistors were not yet a challenge to electron tubes for price or performance even in audio power amplification. By 1968, transistors capable of working at 500 MHz emerged, where as presently, transistors operating upto 10 GHz frequency are available.

The fabrication of high frequency transistors started with the germanium since this material has a larger value of minority carrier mobility and life-time. The maximum operating frequency could not exceed 1 GHz in germanium transistors. However, with the advance in silicon planar technology efforts were switched over to silicon transistors. Present-day transistors utilize thin

silicon epitaxial layers on n^+ substrate, micron photolithography technique and arsenic emitter technology. The two key technological advances which underlie this progress in the art of bipolar transistors are the electron-beam photolithography and the art of very shallow diffusion of both p and n type dopants. Electron-beam lithography is capable of working with geometries having dimensions in the range of .20 μm. Improved base-doping control and profile definition is obtained utilizing ion-implantation and proton-enhanced diffusion. The shallow diffusion of the dopants leads to a heavily doped narrow base accompanied by a steep emitter doping gradient at the emitter-base junction. The introduction of arsenic in recent years as an emitter dopant led to substantial improvement in high frequency performance. Current performance levels of high frequency bipolar transistors available commercially are summerized in Table 1.1.

1.2 Objectives of the Present Work

The survey of literature reveals that the transistor design is still somewhat semi-empirical. There is no general model which can estimate the value of current-gain of high frequency transistors at different injection levels by feeding the material and device parameters, prior to its fabrication.

The present work is concerned with the design and fabrication of a transistor having cut-off frequency near 1 GHz

and with the study of its d.c. common-emitter current gain both theoretically and experimentally. The work was started with the following objectives:

1. Fabrication of high frequency transistors with the available facilities and to find out if line-width of a few microns can be satisfactorily obtained in the laboratory. The other related objective has been to investigate if the shallow diffusion - a characteristic of high frequency transistor, could be performed satisfactorily to obtain a good emitter efficiency and acceptable device characteristics.

2. Study of the common-emitter current gain as a function of injection level and to examine how far the measured results could be explained with the help of the existing analytical models.

3. Investigation of the effect of emitter geometry of the transistor on the cut-off frequency and comparison of the experimental and the theoretical results.

4. Study the effect of emitter geometry on the d.c. performance of the transistors.

A brief account of the work presented in the thesis is as follows:

Chapter 2 describes the design constraints of the high frequency transistors for required performance.

Chapter 3 deals with the fabrication technology of the device. An important technique is the use of arsenic as dopant in the emitter region. Arsenic has been found to yield approximately box type

impurity-profile and the least "emitter-dip" effect.

The measurements made on the device as given in Chapter 4, are the characterization of doping profiles in the base and the emitter regions. The emitter and the base currents have been measured as a function of V_{EB}. The maximum value of h_{FE} and the current carrying capability of the transistors with different emitter geometries have been measured.

In Chapter 5, the maximum value of common-emitter gain $h_{FE_{max.}}$ and the variation of h_{FE} with injection level have been analysed by taking up the measurements of Chapter 4. The dependence of $h_{FE_{max.}}$ and the current carrying capability on the emitter geometry have also been discussed.

Chapter 6 contains the concluding remarks about the present work and also points out the scope for further work.

Table 1.1

Present State-of-the-Art of High Frequency Bipolar Transistors.

Frequency (GHz)	Power output (Watts)	Power Gain (dB)	
1.0	35-40	8-9	
2.0	24	7	
3.0	8	6-7	
4.0	5	5	
5.0	5	6	
6.0	1.5	4	Still in development stage
8.0	1.0	6	
10.0	1.0	4.5	

CHAPTER-2

DESIGN CONSIDERATIONS

Design technique of high frequency transistors is more or less the same as that for low frequency transistors, with the exception that the physical dimensions at high frequency are greatly reduced. This is because the factors which are insignificant at lower frequencies assume major roles at higher frequencies. In fact the designing of high frequency transistors is limited by the technological developments in the field of shallow diffusion, art of photolithography, packaging techniques, improved passivating layers and better metallizing techniques. Hence the available performance of HF transistors depends more on the technology than on the designing skill.

Now-a-days all HF transistors are fabricated in planar form on silicon and are predominantly of n-p-n type. Three types of horizontal geometries have been used in general and are shown in Fig.2.1 [5,6] .

1. Inter-digitated : Used for small signal amplification and power generation.
2. Overlay : Used for power generation only
3. Mesh : Used for power generation only

For continuous high power out-put diamond emitter geometry is frequently used. Here we shall be discussing the inter-digitated

type of geometry only.

2.1 Design Constraints

The performance of high frequency transistors is mainly evaluated in terms of power gain and noise figure [6], both of which have to be optimized in order to get better performance. The other constraints are the output power, the maximum frequency of operation, maximum operating voltages, efficiency and the band-width. These performance parameters are mainly dependant on:

1. The current gain-bandwidth frequency f_T which is the frequency at which short circuit common-emitter current gain of the transistor equals to unity.
2. The junction capacitances and
3. The parasitic resistances of the various regions outside the junction space-charge layer. This includes the base spreading resistance and the resistances associated with the bulk of the semiconductor.

In order to achieve the optimum performance one must air to achieve the following:

1. Current gain - bandwidth frequency f_T should be increased and 2. The parasitic elements should l reduced to their minimum values.

These are the basic requirements for designing the transistors capable of operating at high frequencies. These design parameters will now be discussed in some detail.

finite charging time given by τ_e.

$$\tau_e = r_e \times C_{TE} \qquad (2.3)$$

r_e is given by $\frac{kT}{\eta q} \cdot \frac{1}{I_E}$, where, η is the ideality factor.

B- Base Transit Time

Minority carriers injected from the emitter traverse through the base region by diffusion as well as by drift (in graded base transistors). They take a finite time τ_b to travel the quasi-neutral base region. This transit time can be calculated by defining an equivalent carrier velocity v(x) for the minority carriers. With the knowledge of this velocity the time can be calculated as:

$$\tau_b = \int_0^{W_B} \frac{dx}{v(x)}$$

For an exponential profile τ_b has been estimated as [6].

$$\tau_b = \frac{W_B^2}{2\bar{D}_{nB}(.8+.46n)} \quad \text{for } n \geq 2.5 \qquad (2.4)$$

where, $n = \ln \frac{N_{BE}}{N_{BC}}$ and

$\bar{D}_{nB}$ is the effective value of diffusion constant of minority carriers in the base region. W_B is the base width.

C- Collector Depletion-Layer Transit Time

The velocity of carriers traversing through the reverse biased base-collector junction depletion-region is limited by the saturation velocity. Hence the carriers take significant time to cross this region. This time is given by τ_d as

$$\tau_d = \frac{X_{db}}{2V_{SL}} \qquad (2.5)$$

where, X_{db} = base-collector junction depletion - layer width

$V_{SL} = 6 \times 10^6$ cm sec.$^{-1}$

It has been observed that the step junction equations still apply for the diffused junctions [6].

Hence $$X_{db} \simeq \left[\frac{2\varepsilon_s V_{BC}}{q N_C}\right]^{\frac{1}{2}} \qquad (2.6)$$

where, V_{BC} = base-collector junction reverse-bias voltage.

N_C = doping concentration in the collector region.

ε_s = dielectric constant of the material

D- Collector R-C Charging Time

When the total high resistivity collector region is not entirely covered by the depletion region, it offers a resistance r_c' to the flow of current flowing out of the collector region. Hence the collector junction capacitance is charged through r_c' which takes its own charging time given by

$$\tau_c = r_c' \; C_{TC} \qquad (2.7)$$

where, $r_c' = \frac{L_s}{A_E} \rho_c$

C_{TC} = transition capacitance of the base-collector junction.

L_s = collector substrate thickness not covered by the depletion region.

ρ_c = collector region resistivity

A_E = emitter area.

τ_c can be reduced by using epitaxial wafer such that the base-collector junction depletion region spreads over full epilayer thickness. In that case τ_c becomes negligible in comparison to

where, ρ_1 = average resistivity of the base region just below the emitter region.

ρ_2 = average resistivity of the base region between the emitter edge and the base contact.

In case the number of emitters are more than one, the total base resistance is given by

$$r_b' = \frac{1}{\text{no. of emitters}} \left[r_{b1}' + r_{b2}' + R_C \right] \qquad (2.11)$$

B. Capacitances

During the transit of carriers from the emitter to the collector, they encounter two depletion regions as described above. Each of these depletion regions contributes to a junction capacitance The emitter-base junction capacitance C_{TE} is given by

$$C_{TE} = A_E \left[\frac{\epsilon_s q N_{BE}}{2 (V_{EB} + \varphi)} \right]^{\frac{1}{2}} \qquad (2.12)$$

for silicon,

$$C_{TE} = A_E \times 2.88 \times 10^{-4} \left[\frac{N_{BE}}{2(V_{EB} + \varphi)} \right]^{\frac{1}{2}} \text{ pf} \qquad (2.13)$$

where, A_E = emitter area expressed in cm^2.

N_{BE} = base doping concentration at the emitter edge expressed in cm^{-3}.

V_{EB} = emitter-base junction forward-bias voltage in volts.

and φ = emitter - base junction built-in voltage in volts.

The collector-base junction capacitance C_{TC} is composed of the capacitances C_{CI} of the junction between collector and the base region under the emitter (A_{B1}) and the capacitance C_{CO} of the

junction between the collector and the base region outside the shadow of the emitter (A_{B2}). These capacitances can be determined from Lawrence and Warner Curves [21]. A good approximation for these capacitances is obtained by assuming the base-collector junction to be abrupt. For an abrupt silicon p-n junction these capacitances can be written as:

$$C_{CI} = A_{B1}(cm^2) \times 2.88 \times 10^{-4} \left[\frac{N_C}{(V_{BC}+\varphi)} \right]^{\frac{1}{2}} \quad pf \qquad (2.14)$$

$$C_{CO} = A_{B2}(cm^2) \times 2.88 \times 10^{-4} \left[\frac{N_C}{(V_{BC}+\varphi)} \right]^{\frac{1}{2}} \quad pf \qquad (2.15)$$

where, N_C = collector doping concentration in cm^{-3}.

V_{BC} = base-collector junction reverse-bias voltage in volts.

and φ = base-collector junction built-in voltage in volts.

The values of C_{CI} and C_{CO} calculated using (2.14) and (2.15) were found to be not more than 5% larger than their values read from the Lawrence and Warner curves.

For improved performance these capacitances are aimed at their minimum values. C_{TE} is reduced by reducing A_E and C_{TC} is reduced by reducing the collector doping and the base area.

2.2 Design of High Frequency Transistors

It is clear from the above discussion that the parasitic elements provide feed-back path from the output to input. To achieve the best possible performance it is necessary to minimize this feed-back. The extent to which this feed-back is effective depends on the horizontal as well as the vertical geometry of the transistor.

We shall consider these two dimensions in detail.

2.2.1 Horizontal Geometry

The design begins with the estimation of the emitter periphery. This is decided by the value of the current at desired maximum power gain. In practice the emitter periphery is calculated by assuming a current of 1-2 mA/mil. Next the emitter width is decided by the required maximum operating frequency. This is smaller for higher frequencies. The emitter length-to-width ratio is not allowed to become greater than 20:1 to minimize the voltage drop along the emitter finger.

The base area is decided by the maximum power out-put requirement. Emitter periphery to base area ratio generally called the aspect ratio of the device is higher for larger power out-put.

2.2.2 Choice of the Substrate

The resistivity of the epitaxial layer is estimated by the known values of device operating voltage and the collector-base junction depletion-layer transit time τ_c.

The thickness of the epilayer must be somewhat greater than the depletion-layer width in the collector region, otherwise C_c becomes larger, degrading the performance of the transistor. Moreover, the physical dimensions of HF transistors are in a few microns range, as described earlier. Accordingly, for better yield much surface perfection of the epilayer surface is necessary. Also there must be less inhomogeneities in the bulk crystalline structure and the impurity density in the bulk. To avoid impurity redistribution

in the collector region due to subsequent heat treatments at elevated temperatures, comparatively slow diffusant is preferred during epitaxial growth.

2.2.3 Vertical Geometry

To increase the operating frequency, base transit time has to be reduced and hence the base width is to be kept small. Also to decrease the input charging time, input capacitance and resistance have to be kept low. To achieve these objectives the integral base doping is made higher and the steep doping profile is preferred in the base region. The doping level in the base region cannot be increased much, as it not only reduces the current gain due to increased recombination in the base region, but also causes a decrease in the emitter efficiency [5]. The doping concentration in the emitter region is orders of magnitude higher than that in the base region. This increases the injection efficiency of the emitter region. In order to avoid much compensation of the base doping, an abrupt emitter profile in the vicinity of the emitter-base junction is always necessary. Moreover, compensation in the base region gives rise to a field which opposes the drift of carriers in the base and thus increases the transit time. The emitter being shallow in HF transistors the maximum surface concentration in the emitter region is very much limited by the bandgap narrowing effect [2]. It has been observed that this phenomenon limits the maximum surface concentration in the emitter

to $5x10^{19}$ cm^{-3} for 1 μm and to $9x10^{19}$ cm^{-3} for 2 μm deep emitter-base junction, for the maximum achievable current gain.

2.3 Ohmic Contacts

Platinum silicide is widely used for the front ohmic contact in HF transistors. Initially platinum is deposited on the surface and then silicide is formed by giving the subsequent heat treatment. Aluminium is avoided due to difficulties in getting go ohmic contacts in case of shallow diffused junctions.

The detailed analysis of the geometry of the transistor fabricated for the present work has been given in the Appendix.

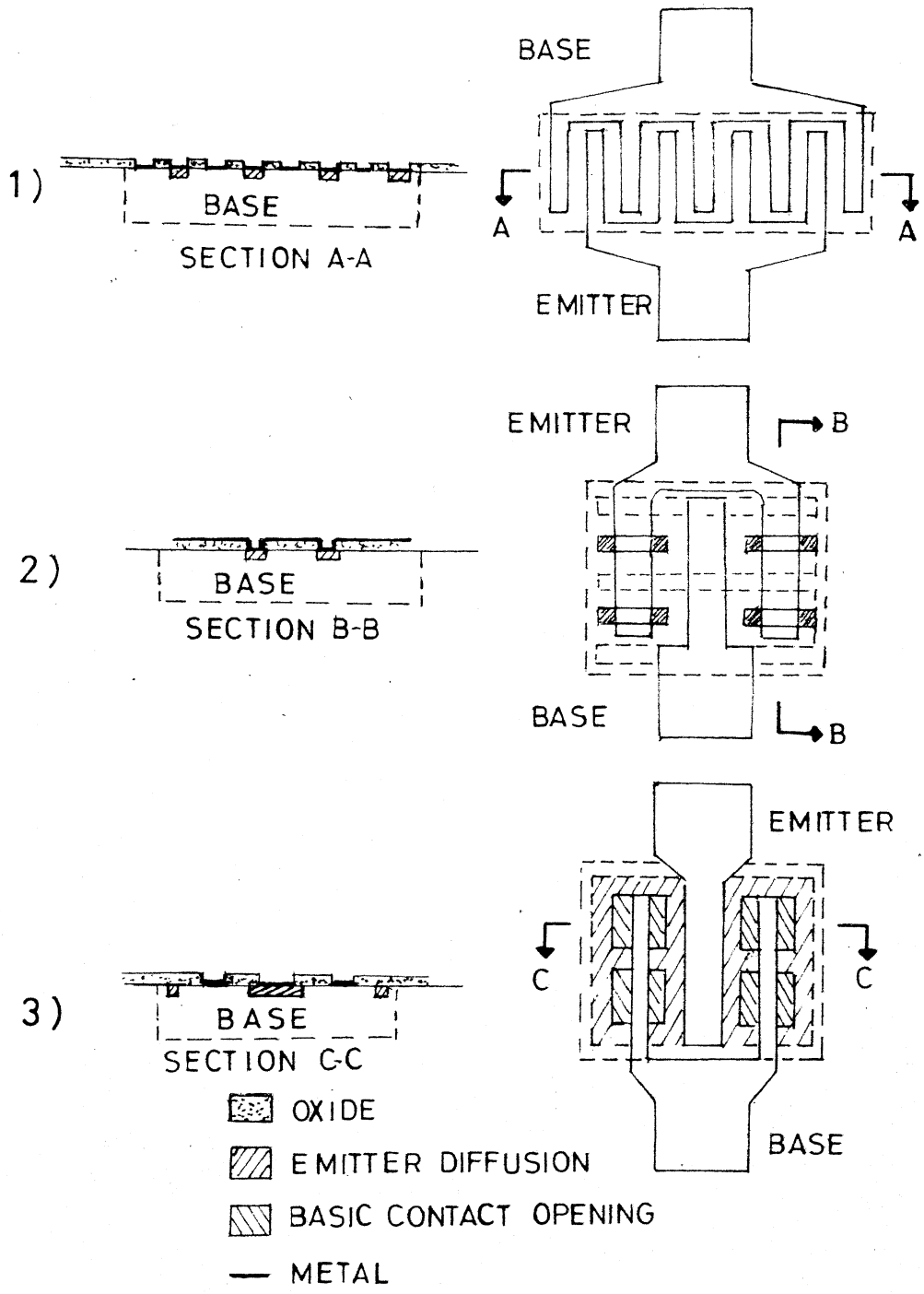


Fig.2-1 Typical High Frequency Transistor Horizontal Geometries

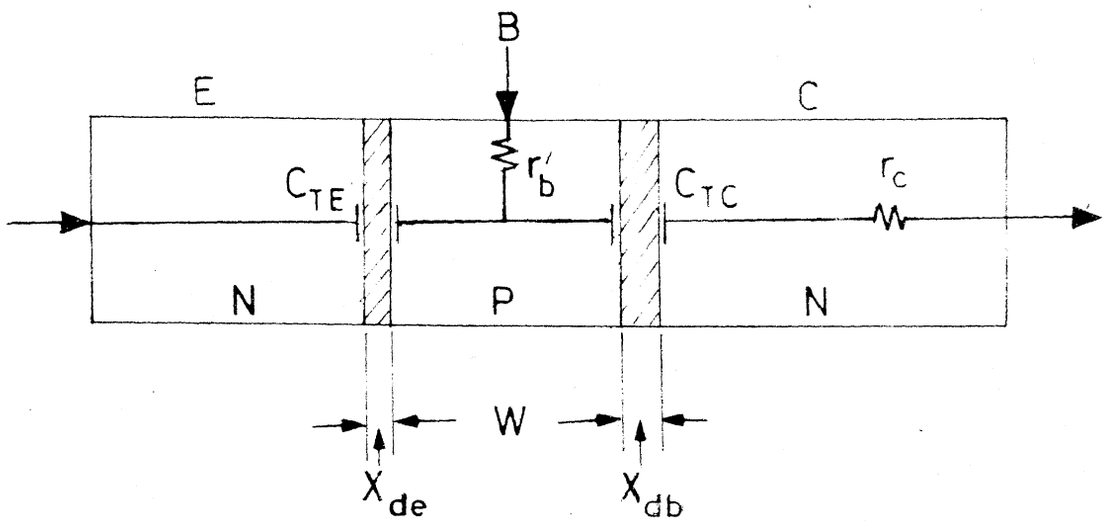


Fig. 2·2 One dimensional view of a junction transistor

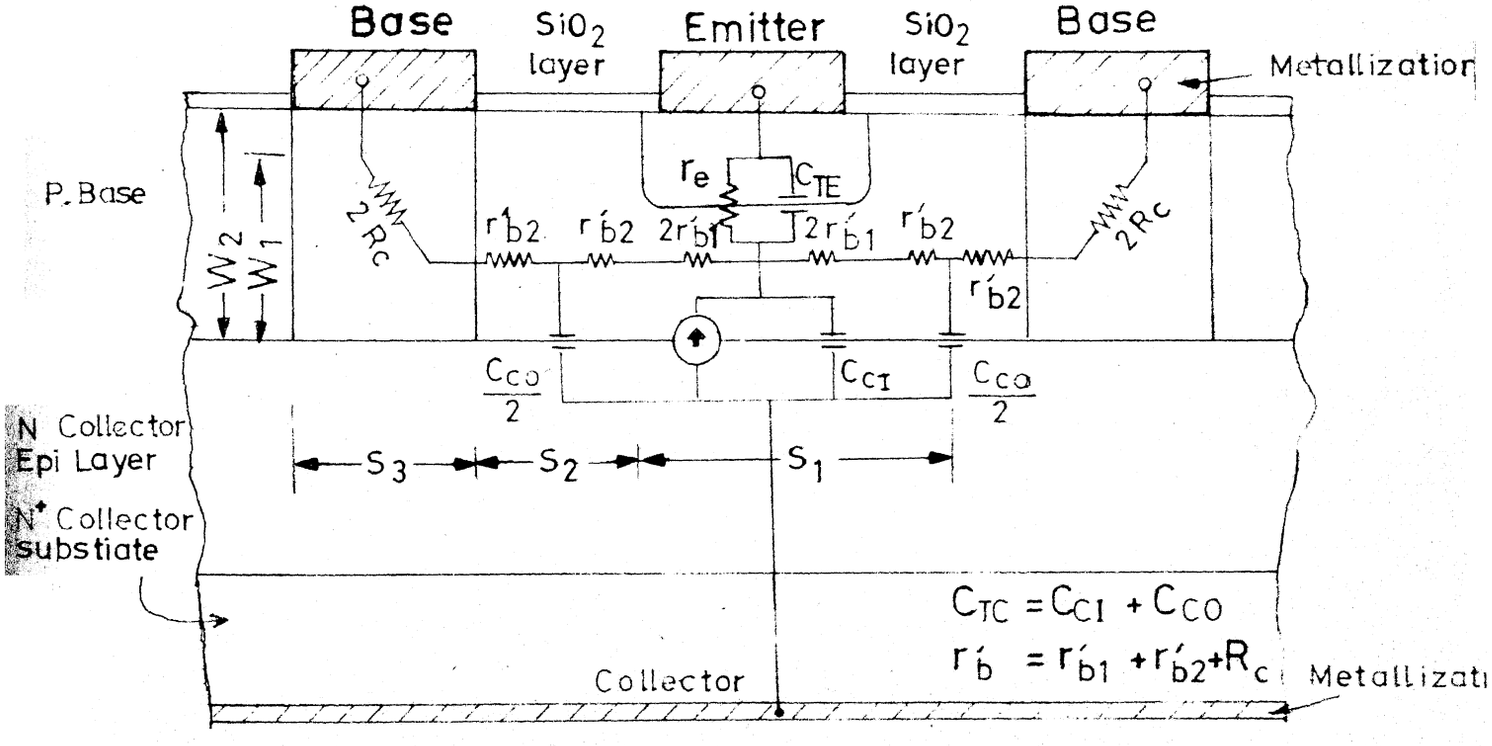


Fig. 2·3 Cross-section of a planar bipolar transistor

CHAPTER 3

FABRICATION TECHNOLOGY

As mentioned in the previous chapter, the performance of high frequency transistors mainly depends on the physical dimensions (both vertical and horizontal) of the device. These dimensions are so much reduced that one finds himself helpless because of the limitations imposed by the processing technology. This is the reason of remarkable improvement in the HF transistors along with the progress of the semiconductor fabrication technology.

One of the most important factors involved in the fabricati techniques is the diffusion technique for a shallow and uniform junct This is because it may well be said that the performance of the HF transistors is determined by the base-width and the impurity distribution in the base region. The cut-off frequency of the transistor increases with the decrease in base-width. To decrease this width, it is necessary to minimize the "emitter dip effect" [20] Arsenic is widely preferred over phosphorous for emitter diffusion because of its lower diffusion constant and closer matching with the silicon lattice [8].

The other important fabrication technique involved is photolithography . In order to meet the fine geometry requirements, the photoengraving technique for fine geometries becomes important.

In the present work, transistors with three different

emitter geometries, as shown in Fig.3.1, were fabricated side by side on an epitaxially grown n-n^+ wafer using double-diffusion proces

3.1 Starting Material

An epitaxial layer grown on single crystal of silicon substrate was taken as starting material. The n^+ type substrate was phosphorous doped, ⟨111⟩ oriented with .002-.007 ohm-cm resistivity. The n-type epilayer ≈.5 μm thick was also phosphorous doped with resistivity .65 ohm-cm and oriented in ⟨111⟩ direction.

To characterize the epilayer surface, stacking fault density was measured by preferentially etching the wafer in Van Sirtl solution [18] for 70 seconds. The stacking fault density was counted to 10,000/cm^2. The etch-pit density was measured by preferentially etching the wafer in the same solution for 4 minutes [18] and was found to be 2000/cm^2.

3.2 Oxidation

A thickness of 0.4 μm of oxide was found to be sufficient to mask against the base diffusion time and temperature requirements [19, 22]. The wafer was cleaned by the usual cleaning procedure [21] and was oxidized under following conditions:

ambient	:	steam
temperature	:	1000°C
time	:	30 minutes
annealing	:	20 minutes at 1000°C in argon ambient at flow rate of 1.3 l/min.

The push-in and pull-out rates were adjusted to about 100°C per minute change in temperature. This was done to avoid mechanical stresses on the wafer due to sudden change in temperature. These mechanical stresses produce mechanical damages at the surface and in the bulk and kill the life time.

The colour of the grown oxide was red-violet which corresponds to .46 μm thickness as seen from the colour-oxide thickness chart [21].

3.3 Photoengraving

3.3.1 Surface Preparation

As the present geometry was fine, extreme care had to be exercised for ensuring surface cleanliness and conditions for better photoresist adhesion [10, 11, 12]. The wafer was cleaned twice by ultrasonic cleaning in DI water. It was then boiled in trichloroethylene (TCE), acetone and methanol successively for five minutes each and rinsed in DI water thoroughly. Next it was boiled in HNO_3+H_2SO_4 + DI water (1:1:1 by volume) solution for 10 minutes and rinsed thoroughly in DI water followed by silane treatment [10].

Silane Treatment

Two solutions were prepared with the following compositions:

solution no.(1) : TCE & Dichloro Dimethyl Silane (100:3 by volume)

solution no.(2) : TCE & Isopropyl alcohol (1:1 by volume)

The wafer was dipped in solution no.(1) for about 50 seconds and

then rinsed in solution no.(2) for about 50 seconds. This treatment was repeated until the surface was hydrophobic. Then the wafer was kept in oven for 40 minutes at 200°C in inert (nitrogen) ambient. This dries-off any traces of moisture on the surface.

3.3.2 Photoresist Coating

KTFR and KTFR thinner were mixed in 1:2 ratio by volume. The solution was prepared about a day prior to use, for the proper mixing of its two constituents [11]. The prepared solution was spun on the prepared surface of the oxidized wafer through a .8 μm filter, at 6000 rpm for 20 seconds. When the first layer of the photoresist dries-off, another layer was coated at the same speed. This minimises the chances of pin hole formation [22]. Next the photoresist coated sample was prebaked at 85°C for 18 minutes in nitrogen ambient. During prebaking the traces of solvent in the photoresist are driven out.

3.3.3 Pattern Delineation in Photoresist

The first mask was aligned to the wafer so that the window edges were parallel or perpendicular to the cutting direction of the wafer. This helps in dicing the wafer in final stage. A time period of 20 seconds was used for the exposure to ultraviolet radiation. The exposed slice was developed and then rinsed in commercially available KTFR developer and rinse respectively. The developing and rinsing times were 2 minutes each.

After drying the slice, it was observed under unitron microscope for correct mask registration and the opening of windows in photoresist. Then the sample was post-baked at 155°C for 25 minutes in nitrogen ambient. Post-baking improves the adhesion between photoresist and the oxide surface.

3.3.4 Oxide Delineation

This was done in buffered HF (48% HF & 40% NH_4F in 1:5 ratio by volume). The etching time was first determined on a test sample, then the actual sample was delineated for about two minutes more than it takes on the test sample, to ensure complete oxide etching. Extreme care was taken to avoid undercutting, by dipping the sample in buffered HF till whole of the oxide is removed. Once the sample is taken out of the BHF, it is not advisable to dip it again to remove the remaining oxide if any. This leads to heavy under-cutting. Moreover, the oxide surface is not stressed mechanically (like swabing to clean the surface) before photolithography. This also gives rise to under-cutting [22].

The time taken to delineate the oxide (0.4 μm) on actual sample was 7 minutes.

After the delineation was over, the sample was thoroughly rinsed in DI water. Then the exposed photoresist was removed by boiling the sample in photoresist stripper for 10 minutes. It was then rinsed in DI water, dried up and observed under microscope for the under-cutting, registration and edge sharpness of the delineated windows.

After the above inspection, the wafer was ready for base diffusion.

3.4 Base Diffusion

The base diffusion was aimed to get a gaussian profile with surface concentration of 10^{18} cm^{-3} and junction depth of 1.5 μm. Boron-Nitride wafer is the appropriate boron sourse to obtain uniform sheet resistance and reproducibility [9]. The steps in the base diffusion were as follows:

3.4.1 BN Wafer Surface Activation and Stabilization [3]

BN wafer was first cleaned by ultrasonic cleaning in TCE twice. It was then boiled in TCE and acetone respectively for 5 minutes each, followed by thorough rinsing in DI water. Next, the surface was etched in buffered HF for 40 seconds and rinsed in DI water thoroughly. Finally, it was rinsed in DDI water and was dried at the mouth of the diffusion furnace for 30 minutes. The ambient was nitrogen at the flow rate of 600 cc./minute.
To reactivate the cleaned BN wafer surface, it was pushed inside the diffusion furnace under following conditions:

furnace temperature	:	930° C (same as pre-deposition temperature)
ambient	:	Oxygen at the flow rate of 600 cc/min.
time	:	20 minutes

After the activation step, the surface was stabilized by changing the ambient of the furnace from oxygen to nitrogen at the same flow rate and at the same furnace temperature. The stabilization time was 25 minutes.

While using BN wafer, the main precaution observed was that a platinum piece was kept in the quartz boat slot to avoid direct contact of BN wafer with the boat. If the BN wafer is allowed to come in direct contact with the boat material it forms borosilicate glass which results in sticking of BN wafer to the boat.
A quartz sleeve was also used around the boat to avoid the diffusion of boron-nitride particles, emitted by BN wafer, into the diffusion tube.

3.4.2 Predeposition

The delineated sample was first cleaned in solvents and then etched in 7% HF for 30 seconds to remove any oxide that may form during its storage in the atmospheric ambient. It was decanted in DI water followed by decanting in DDI water. The sample was loaded into the diffusion furnace tube in the boat in such a way that it was parallel to the BN wafer. BN wafer was facing the gas flow and silicon wafer was in full shadow of it.

Predeposition conditions were as follows:

temperature	:	930°C
ambient	:	nitrogen at a flow rate of 600 cc/min.
		+ oxygen at a flow rate of 50 cc/min.
time	:	12 minutes.

Distance between BN wafer and the sample was 125 mils.
Push-in and pull-out times were about 7 minutes each. A test sample was also pre-deposited under exactly the same conditions

as above, for evaluating the base diffusion profile.
After the predeposition was over the wafer was etched in 7% HF for 1 minute to remove the borosilicate glass layer deposited on the wafer surface during pre-deposition. It was then decanted in DI water thoroughly, followed by a decant in DDI water.

3.4.3 Drive-in Diffusion

The drive-in diffusion was performed in an oxidizing ambient to grow oxide simultaneously, for the purpose of masking the sample surface against emitter diffusion [24]. The whole drive-in diffusion time was properly divided in dry steam-dry cycle according to the oxide thickness requirement.
For masking against emitter diffusion 0.5 μ oxide thickness was found to be sufficient. Drive-in diffusion cycle was as follows:

I ambient : dry oxygen at a flow rate of 1.5 l/m
temperature: 1100°C
time : 15 minutes

II ambient : steam
temperature: 1100°C
time : 20 minutes

III ambient : argon at a flow rate of 1.5 l/m
temperature: 1100°C
time : 15 minutes

push-in and pull-out times were typically about 10 minutes each.

After the drive-in diffusion emitter windows were delineated by following the same steps as in section 3.3. The oxide layer to be delineated here was doped oxide layer. The etching rate of the doped oxide is larger than that of the undoped oxide. Thus to get the sharp edge definitions, a slow etchant was preferred [10]. Buffered HF with 1:6 composition was used for window delineation which took 6 minutes to completely etch out the oxide layer.

3.5 Emitter Diffusion:

Arsenosilica film is one of the widely used dopant sources for emitter diffusion in high frequency transistors [8]. After the usual wafer cleaning in solvents, the wafer was boiled in H_2SO_4 + HNO_3 + DI water (1:1:1 by volume) solution for 10 minutes. This resulted in a very thin layer of oxide of the order of a few Angstroms. The oxide layer improves the adhesion of arsenosilica film to the sample surface, particularly in the emitter window region. The wafer was then rinsed in DI water thoroughly followed by rinsing in DDI water.

The arsenosilica film with the maximum dopant density of 10^{20} cm^{-3} was spun on the clean and dry sample surface using photoresist spinner at 3000 rpm for 20 seconds. The sample was then baked in an oven at 220°C in a nitrogen ambient for 20 minutes. A coating of silica film was done at 4000 rpm for 20 seconds and again it was baked at 220°C in nitrogen ambient for 20 minutes [13]. Silica film was coated over arsenosilica film to serve as a mask for diffusion of phosphorous into the sample from phosphorus

contaminated diffusion furnace tube.

After the two films were deposited onto the sample surface, it was loaded into the diffusion furnace when its temperature was 600°C and the ambient was nitrogen at a flow rate of 1.0 l/minute. Now the temperature of the furnace was raised to 1150°C slowly in 20 minutes.

The diffusion time was 35 minutes.

Post- iffusion Heat Treatment

After the diffusion was over the diffused sample was given heat treatment at a lower temperature. At lower temperatures around 700°C, the in-diffusion becomes negligible and the sheet resistance of the diffused layer increases because of out-diffusion from the wafer [8] , resulting in flattening of the diffusion profile from gaussian distribution towards box distribution.

The post-diffusion heat treatment was done at 700°C for 1 hour in nitrogen ambient with a flow rate of 1.0 l/minute.

A p-type (.2-1 ohm-cm) test sample which was used to evaluate the emitter diffusion profile was placed alongwith the actual sample.

3.6 Back Surface Preparation

It was observed that during the base diffusion some boron diffusion occured at the back side also,which gave rise to a rectifying junction on that side. A thin layer of silicon was removed from the back side by lapping it with a 14.5 µm abrasive for about 2 minutes while the front side was protected by coating

it with black wax.

3.7 Contact Opening

The oxide thickness to be delineated here was nearly .5 μm contributed by the two layers of silica films deposited on the sample surface. The emitter contact openings had dimensions in few microns range, therefore to get sharp edge definitions, it was necessary to reduce the oxide thickness [10] prior to perform the photolithography. Moreover, this oxide layer acts as an insulation between metal pads (for bonding purpose) and the silicon surface. Therefore a thin layer of oxide of the order of .2 μm is sufficient.

To reduce the thickness of the oxide layer, it was etched in 7% HF for 3 minutes. The sample was rinsed in DI water and subjected to the same steps as given in section 3.3.

Buffered HF with 1:6 composition took 4 minutes to delineate the contact windows.

3.8 Metallization and Contact Etching

Suitable metals were evaporated to make ohmic contacts with the emitter, base and the collector regions through contact openings.

3.8.1 Metallization

Gold was evaporated for back contact whereas aluminium was used for front metallization. Before doing the front metallization the silicon substrate was heated on a substrate heater inside the vacuum chamber at about 220°C for about 12 minutes. Typical

pressure before the evaporation was 2×10^{-5} torr which increased to 4×10^{-4} torr during evaporation. Aluminium thickness was kept about 1000 Å. Emitter-base junction being shallow sintering was avoided, because aluminium was found to diffuse fast shorting the emitter-base contact.

3.8.2 Metal Etching

Final step of photolithography was done on the metallized surface. This resulted in a metal contact strip from the emitter and the base regions extended upto the respective bonding pads. It is necessary to mention the photo-engraving steps again, as the photoresist and surface preparation requirements were entirely different from those that were used for oxide delineation. The photolithography steps were aimed at the easy removal of the photoresist from the metallized surface. The removal of photoresist is necessary to ensure proper bonding between the metal and the bonding leads. Moreover, it was found that even for fine geometries aluminium etchant does not require very good adhesion between the photoresist and the metal surface. The photoresist was prepared in 1:2 (1 part KTFR : 2 parts KTFR thinner, by volume) ratio. The prepared photoresist was coated, using .8 μm filter, at 6000 rpm spinner speed for 20 seconds. One coating of photoresist was convenient from the mask alignment point of view. When a thick layer of photoresist was used, it was difficult to see clearly the geometry under the metal layer. The photoresist coated wafer

was prebaked at 60°C for 10 minutes in a nitrogen ambient. After mask alignment it was exposed for 10 seconds to the ultraviolet radiation . Developing and rinsing times were 2 minutes each. The developed wafer was post-baked at 100°C for 15 minutes after observing under microscope for correct mask registration.

The etchant used had the following composition:

Ortho-phosphoric acid	:	45 cc
glacial acetic acid	:	36 cc
nitric acid	:	2.2 cc
DI water	:	18 cc

The etchant was heated at 60°C during etching, to increase the etching rate. The proper etching time was found 6 minutes.

A photographic reproduction of the typical set of fabricated transistors with three different emitter geometries, as seen on a microscope screen, is shown in Fig.3.2. This is 100 times magnified view of the actual device.

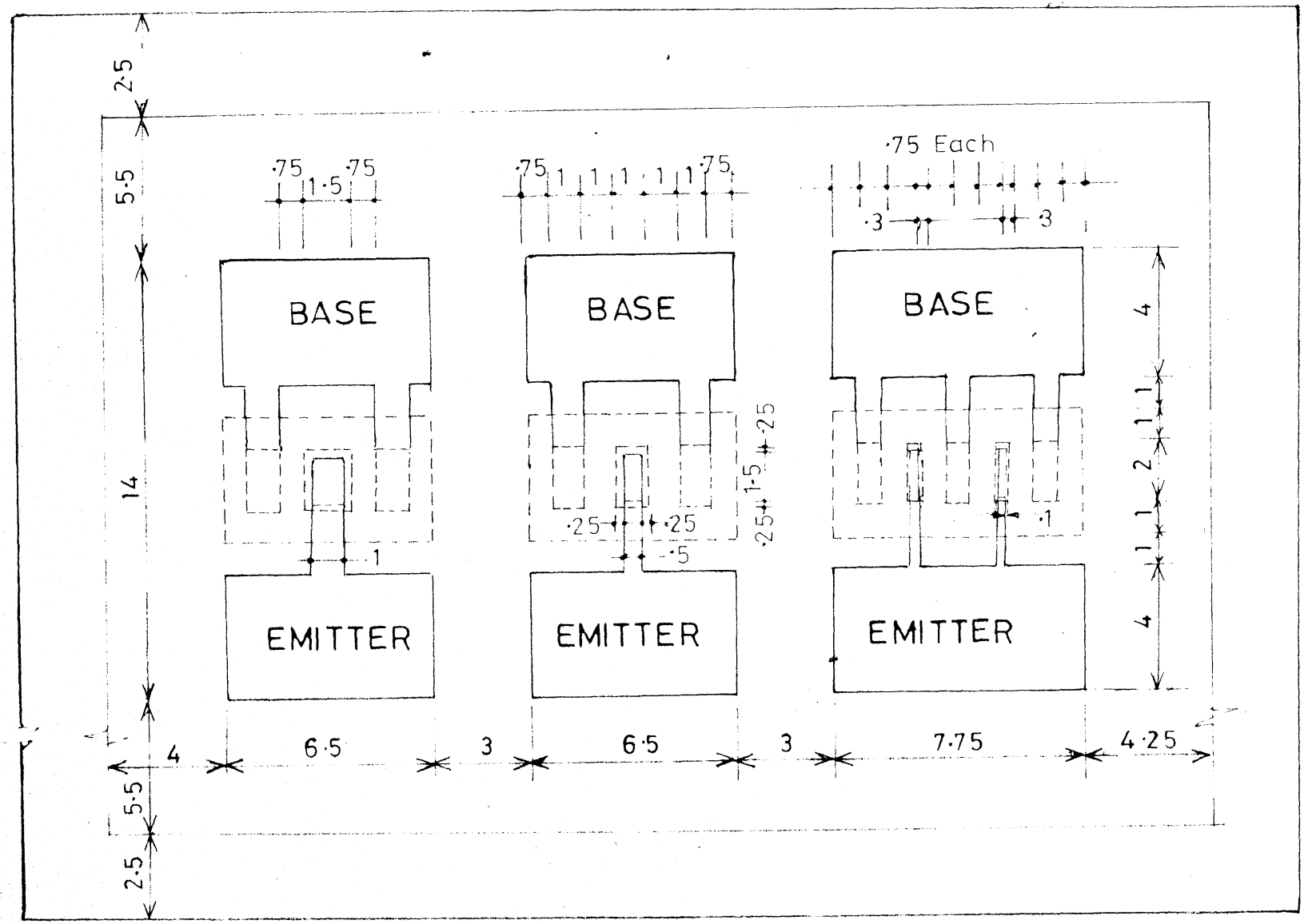


Fig. 3·1 Horizontal geometry of three transistors fabricated
(All dimensions in mils)

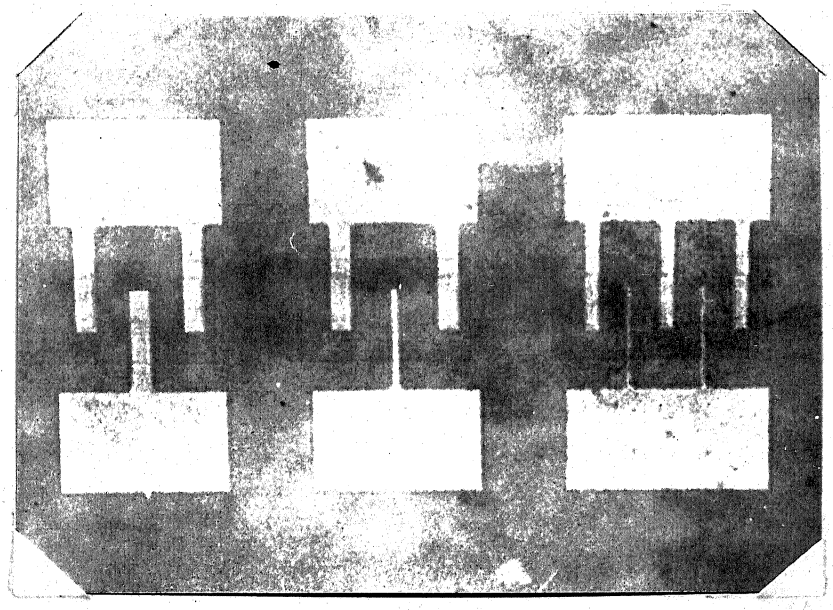


Fig. 3.2 Photograph (1x100) of a Typical Set of Fabricated Transistors with Three Different Emitter Geometries.

CHAPTER 4

DETERMINATION OF DOPING PROFILES AND MEASUREMENT OF D.C. PARAMETERS

In the first two chapters we have discussed the parameters that interact to control the common-emitter current gain in high frequency transistors. The most significant of these parameters are the emitter surface concentration, the maximum doping level in the base region, doping profiles in the base and the emitter regions and the base-width. Among these the emitter surface concentration is the most critical parameter particularly in the shallow junction transistors where the total emitter thickness is comparable to the diffusion length of the minority carriers in the emitter region. The injection efficiency in the high frequency transistors cannot be increased much by increasing the emitter surface concentration because of the dominant bandgap narrowing effect beyond 10^{17} cm^{-3} [1]. These parameters therefore were determined experimentally.

4.1 Measurement of Junction Depths

The emitter-base and the base-collector junction depths were measured on the test samples, using the angle lap and staining technique [18]. The emitter-base junction depth was found to be 1.2 μm and the base-collector junction was 1.5 μm deep, giving a base width of .3 μm.

4.2 Evaluation of Doping Profiles

The impurity distributions in the emitter and the base regions were determined by the technique of successive removal of a thin layer of silicon and subsequently measuring the sheet resistance.

For the successive removal of silicon layer, a thin layer of oxide was grown by anodic oxidation method and the grown oxide was removed by dissolving it in hydrofluoric acid.

The sheet resistance was measured using the four-point probe technique.

The bulk resistivity $\rho(x)$ was determined from the sheet resistance $\rho_s(x)$ using the following relation [15]-

$$(x) = \frac{0.4343\ \rho_s(x)}{\frac{d}{dx}\left[\log_{10} \rho_s(x)\right]} \qquad (4.1)$$

$\log_{10} \rho_s(x)$ was plotted as a function of x on a linear graph. The slope of the tangents at different points were evaluated, giving the slope $\frac{d}{dx}\left[\log_{10} \rho_s(x)\right]$.

The impurity concentration corresponding to each value of $\beta(x)$ was obtained from Irvin's concentration vs resistivity curves [22].

4.2.1 Emitter Profile

The sample was cleaned in solvents and the surface sheet-resistance was measured. Initial weight of the sample was measured on a micro-balance. Then the sample was subjected to

anodic oxidation.

The solution with the following composition was used as an electrolytic solution for anodic oxidation:

0.1N solution of potassium nitrate in ethylene glycol	= 100 cc.
DI water	= 7 cc.

The appropriate value of the anodic cell initial voltage was determined after repeatedly performing the oxidation process till a uniform layer of oxide was achieved. This was found to be 120 volts. The current through the solution at this voltage was 20 mA which decayed to 6mA as a thin layer of oxide was grown. The current was again increased to 80 mA and the oxidation process was arrested when the current reduced to 6 mA.

A uniform oxide layer of metallic-yellow colour was observed which corresponds to an oxide thickness of about .20 microns.

After performing thirteen cycles of anodic-oxidation, when whole of the n-type material is removed, the final weight of the sample was measured. The difference between the initial and the final values of the weight reveals that 920A° thick silicon layer was removed in each cycle of anodic-oxidation

The resulting emitter-impurity profile, as evaluated on a typical test-sample, is shown in the plot of Fig.4.1.

4.2.2 Base Profile

The same steps, as described above, were executed on a

test sample for evaluating the base profile. The initial voltage of anodic cell for the growth of uniform oxide layer was found to be 100 volts. The initial current through the electrolytic solution at this voltage was 20 mA, which decayed to 4 mA as a thin layer of oxide was grown. The current was again increased to 20 mA and the oxidation was arrested when the current reduced to 4 mA.

A uniform oxide layer of light-blue colour was observed which corresponds to about .15 micron thick oxide.

Whole of the p-type layer was found to be removed after performing 20 cycles of anodic oxidation. The difference between the initial and final values of the weight of the sample reveals that 747.5A° thick layer of silicon was removed during each cycle of anodic oxidation.

The base-impurity profile, as evaluated on a typical test-sample is shown in the plot of Fig.4.1.

4.3 Junction I-V Characteristics

The oscillographic reproduction of the current-voltage characteristics of the emitter-base and the base-collector junctions for a typical device (geometry (1)) are shown in Figs.4.2 and 4.3 respectively.

The current at 3 volts reverse-bias was 0.32 μA for the emitter-base junction and 0.60 μA for the base-collector junction.

The forward resistance at 5 mA current was evaluated as 450 ohms for the emitter-base junction and 250 ohms (at 5 mA current)

for the base-collector junction.

4.4 Set of V_{CE}-I_C Curves of a Typical Transistor

The set of V_{CE}-I_C curves for a typical device (geometry (1)) in common-emitter configuration, as seen on an oscilloscope, are reproduced in Fig.4.4. The increase in common-emitter current gain h_{FE} with increase in V_{CE} can be visualized by the slope of the curves.

The decrease in h_{FE} at high injection levels can also be seen clearly by the crowding of the curves as I_c increases.

4.5 Measurement of I_B and I_E as a Function of V_{EB}

The emitter and the base d.c. currents were measured as a function of emitter-base junction forward bias, keeping the base-collector junction reverse bias at 5 volts. The circuit arrangement for the measurements is shown in Fig.4.5. Enough care was taken to keep the base-collector junction reverse-bias voltage constant, which may change during measurements due to high injection effects.

The voltages were measured with a maximum error of $\pm$ .001% upto 1 volt range and $\pm$.01% in greater than 1 volt range. The respective error in the current measurement was $\pm$0.5% throughout the measured range.

The d.c. common-emitter current gain (h_{FE}) was evaluated at different injection levels using the relation $h_{FE} = \frac{I_C}{I_B}$.

A semilog plot of I_c vs V_{EB} for a typical device (geometry (1))

is shown in Fig.4.6(a). The slope $\frac{d(\log I_C)}{dV_{EB}}$ of this curve was evaluated, giving the value of the expression $\frac{kT}{\eta q}$, where, η is the ideality factor. The value of ideality factor was found to be 1.095. Its value starts increasing after the emitter-current level reaches to 10^{-4}A, which corresponds to a current density of $5.17 A/cm^2$.

Fig.4.6(b) shows the variation of the base current I_B with V_{EB}. The base current increases exponentially with $\frac{V_{EB}}{V_T}$ ($V_T = \frac{kT}{q}$) for $V_{EB} > 0.5$ volts. After the base-current reaches to about 10^{-2} mA, the exponential relation of I_B with $\frac{V_{EB}}{V_T}$ is no more seen due to the dominant effect of the base spreading resistance.

The current-gain h_{FE} has been plotted as a function of the emitter current as shown in Fig.4.6(c). It is observed that the gain increases with I_E till the emitter current reaches a value of 4×10^{-4}A. After this the value of h_{FE} becomes almost constant and remains so upto an emitter current of 10^{-2}A. The emitter currents 4×10^{-4}A and 10^{-2}A correspond to $20.67 A/cm^2$ and $516.66 A/cm^2$ current densities respectively.

As the emitter current is increased further, the gain h_{FE} decreases sharply as the high injection effects start dominating.

The above measurements were taken for the geometries (2) and (3) also. The results are plotted in Figs.4.7 and 4.8 respectively.

These devices show similar behaviour as observed for geometry(1) and no significant difference is visible.

4.6 Measurement of $h_{FE_{max.}}$ and the Current-Carrying Capability of the Transistors

The dependence of the maximum value of the common-emitter current gain $h_{FE_{max.}}$ on the emitter periphery to emitter area ratio and the effect of emitter periphery to base area ratio on the current carrying capability of the high frequency transistors were studied.

For this study transistors with three different emitter geometries were fabricated side by side to avoid any variation of parameters due to changes in process variables or wafer inhomogeneities within the three geometries.

The measured values of $h_{FE_{max.}}$ for a typical set of three transistors with different emitter geometries are listed in Table 4.1.

The current carrying capability of these transistors was also measured on the same set of devices and the results are listed in Table 4.1.

Table 4.1

$h_{FE_{max.}}$ and Current-Carrying Capability Measurements

	$\frac{\text{emitter-periphery}}{\text{emitter-area}}$	$h_{FE_{max.}}$	$\frac{\text{emitter-periphery}}{\text{base-area}}$	Current-Carrying Capability
Geometry(1)	.0908	32.4	.01184	1250A/cm^2
Geometry(2)	.1167	38.8	.01020	1025A/cm^2
Geometry(3)	.1946	40.2	.01255	1700A/cm^2

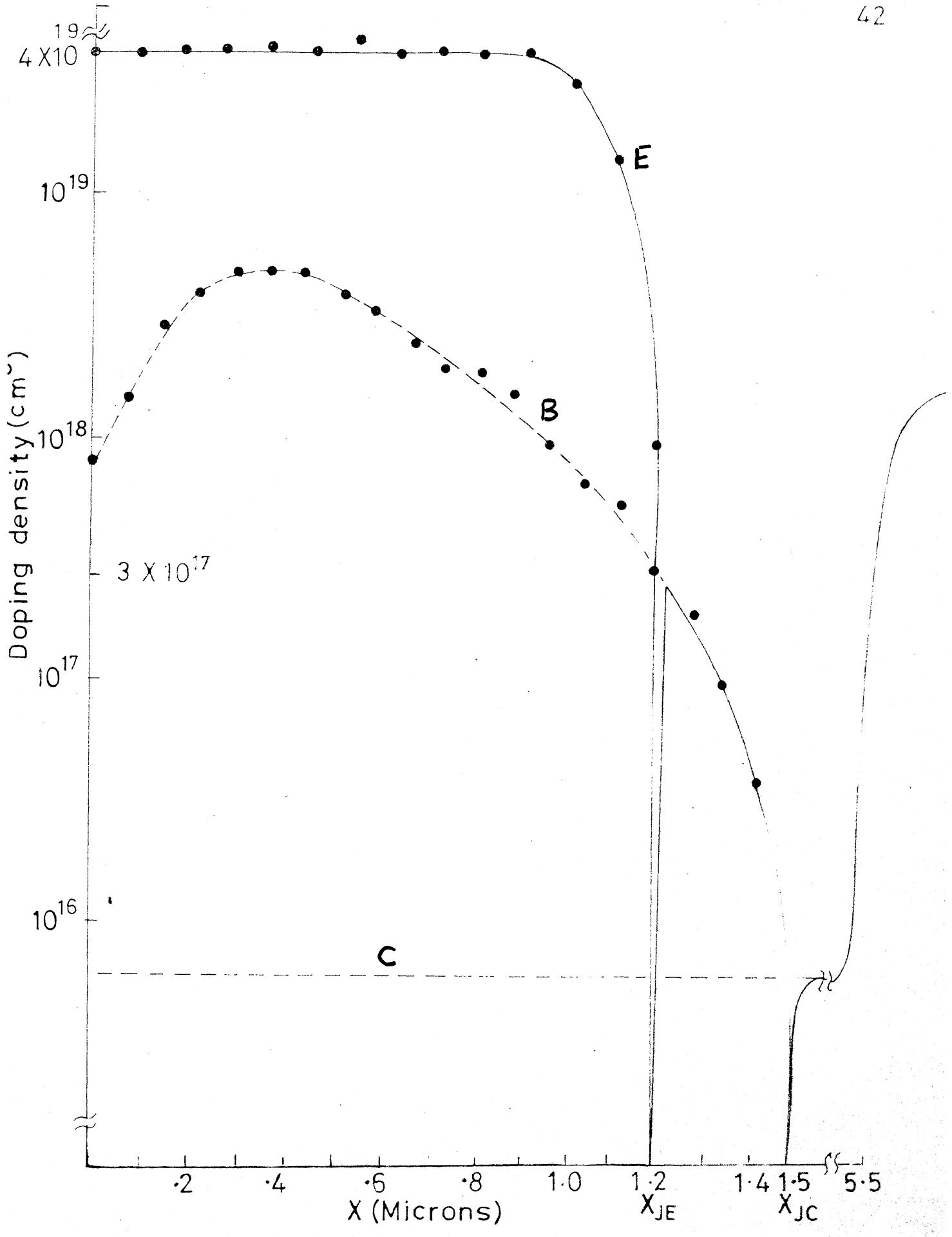
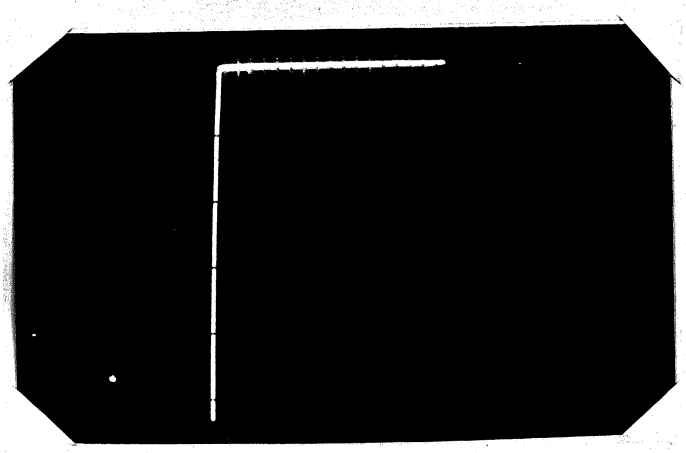
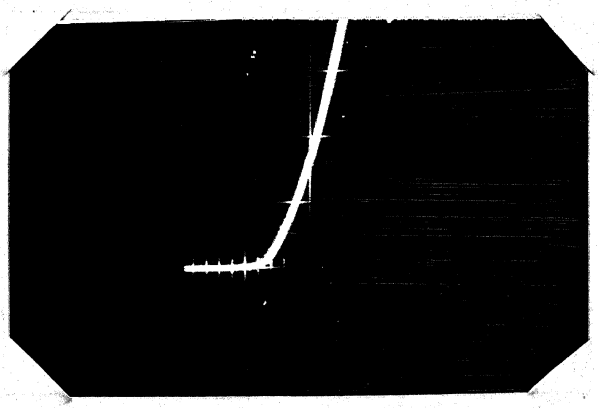


Fig. 4·1 Plots of Typical Doping Profile in Various Regions of the Transistor.

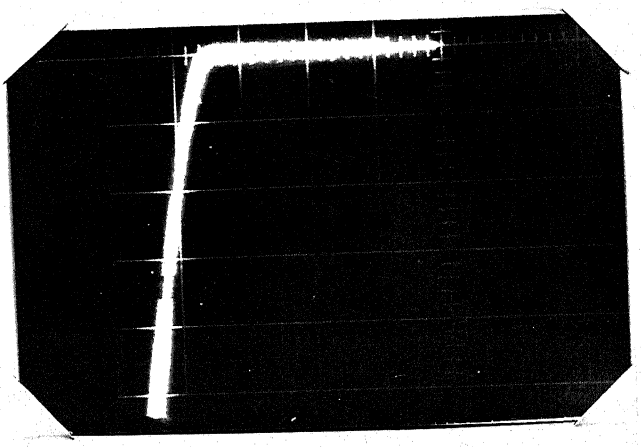


Reverse Characterstics
X-axis Voltage (2V/Div.)
Y-axis Current (.05mA/Div.)

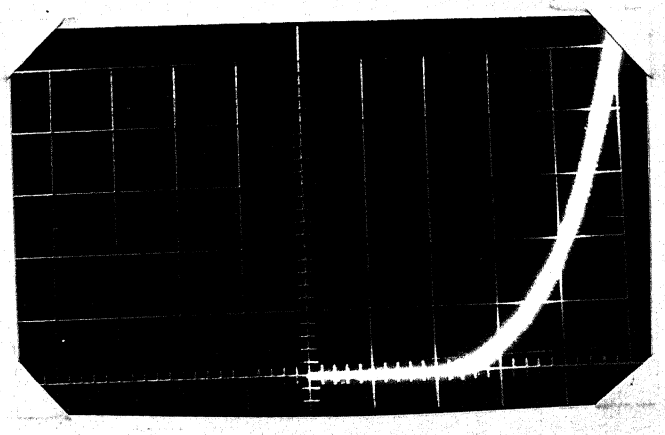


Forward Characterstics
X-axis Voltage (.5V/Div.)
Y-axis Current (.05mA/Div.)

Fig. 4.2 Emitter-Base Junction I-V Characterstics of a Typical Transistor.



Reverse Characterstics
X-axis Voltage (5V/Div.)
Y-axis Current (.05mA/Div.)



Forward Characterstics
X-axis Voltage (.2V/Div.)
Y-axis Current (.05mA/Div.)

Fig. 4.3 Base-Collector Junction I-V Characterstics of a Typical Transistor.

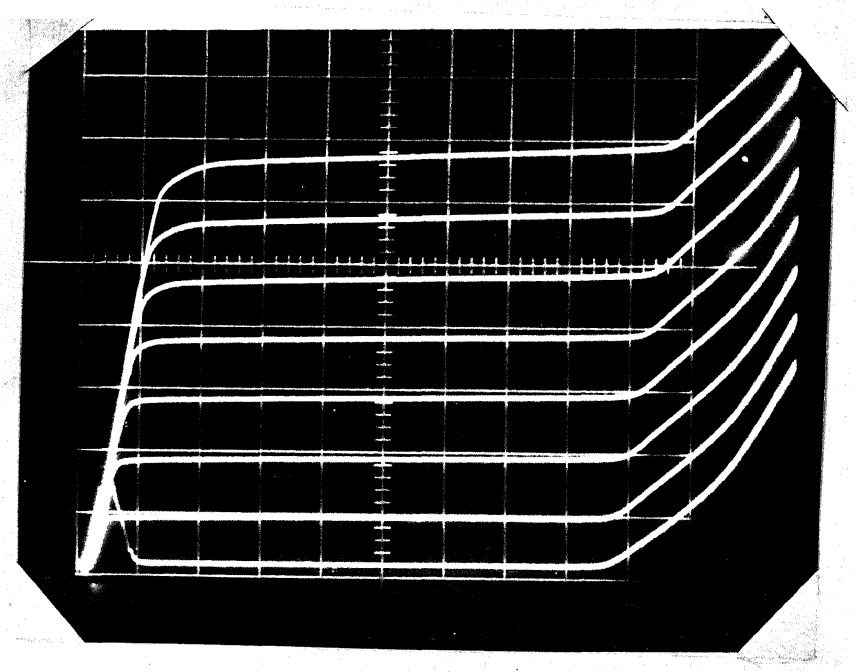


Fig.4.4: Set of V_{CE} - I_C Curves for a Typical Transistor Geometry(1).
X-axis V_{CE} (2V/Div.)
y-axis I_C (2mA/Div.)
Base current I_B = .05mA/Step.

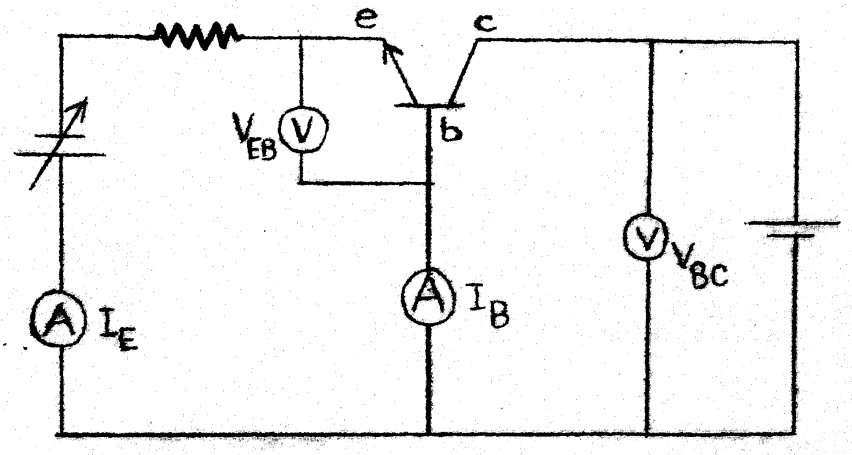


Fig.4.5: Circuit arrangement for the measurement of I_B and I_E as a function of V_{EB}.

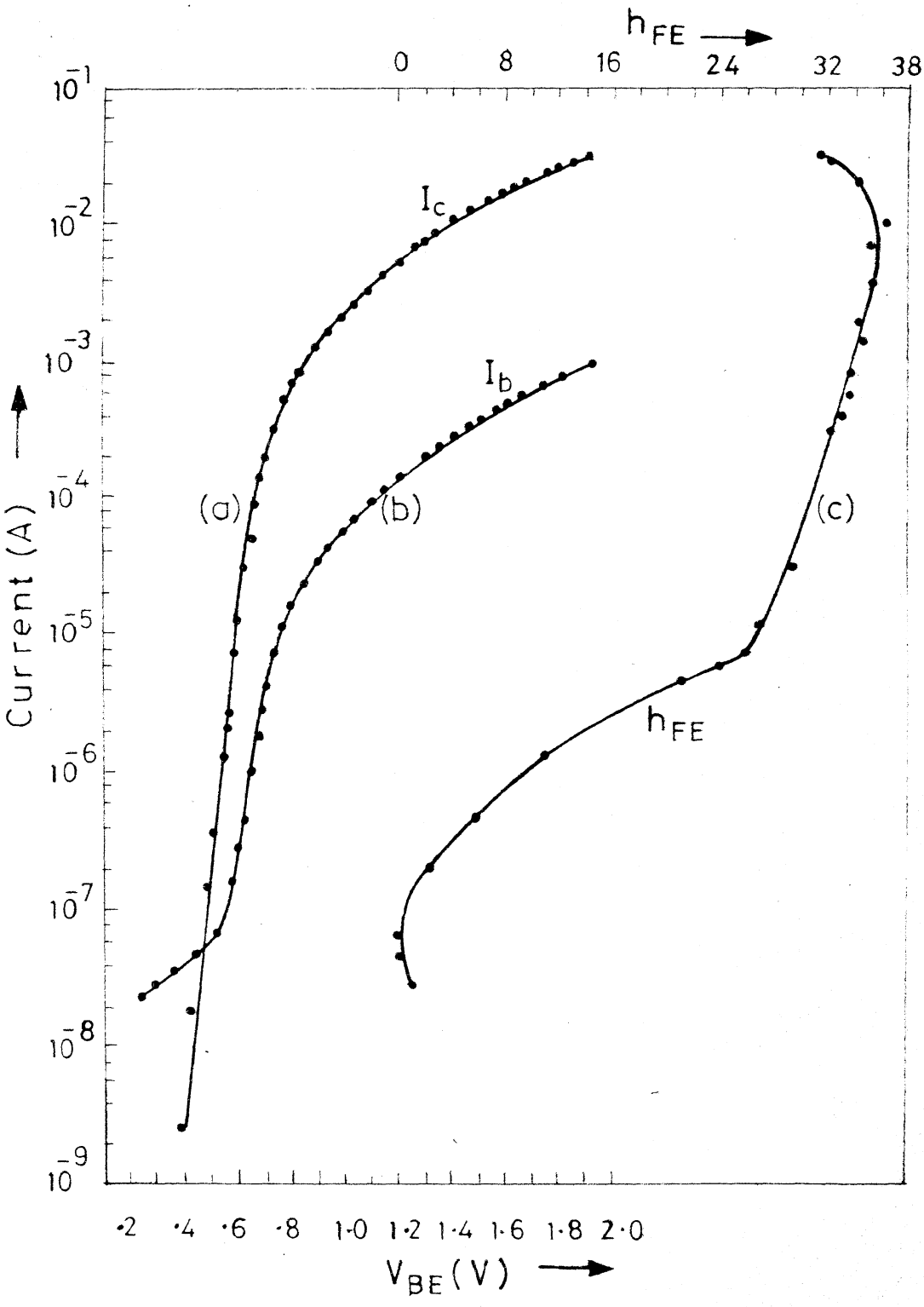


Fig. 4-6 Plots of I_C and I_B vs V_{BE} and h_{FE} vs I_E for a Typical Transistor Geometry (1)

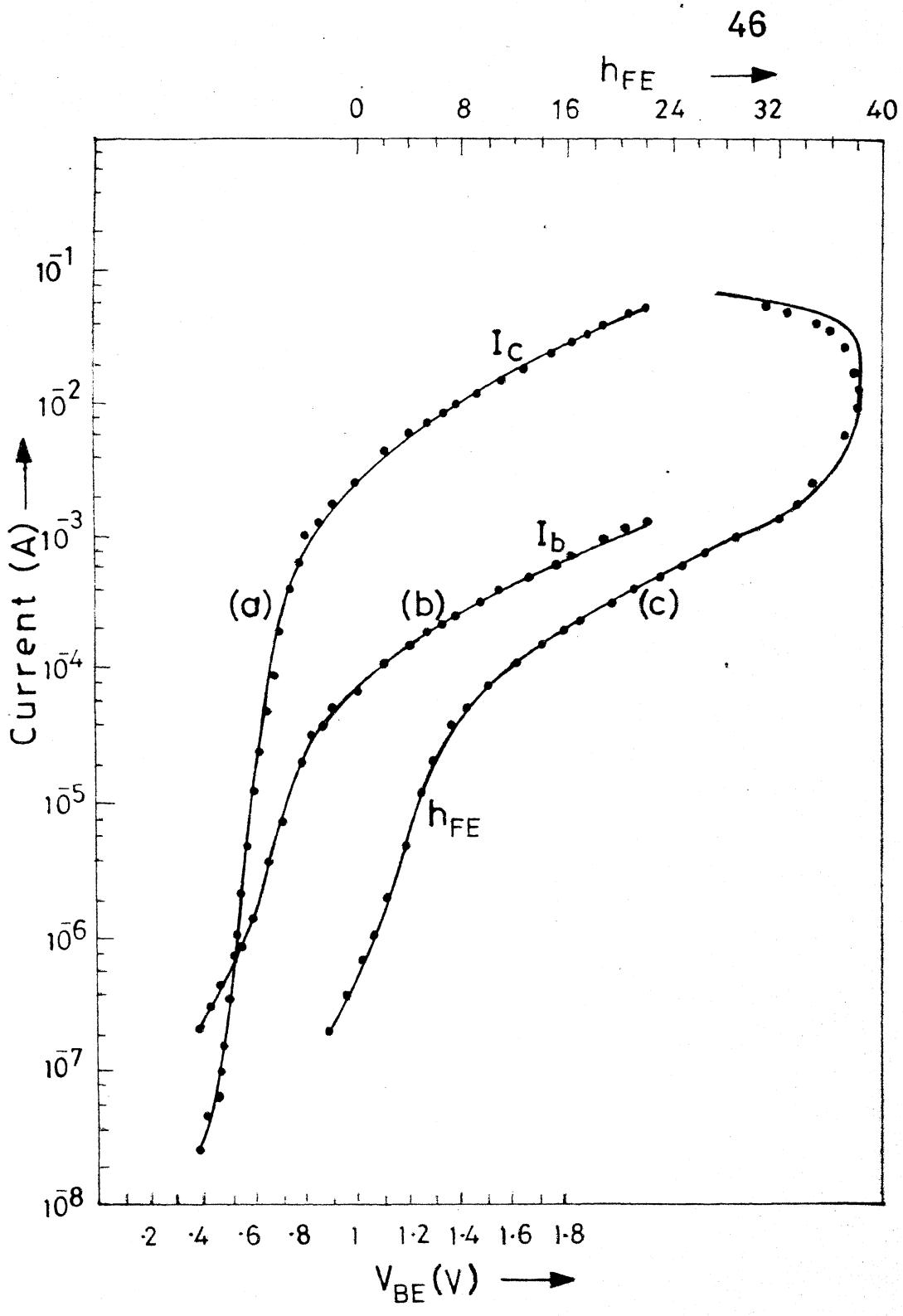


Fig.4·7 Plots of I_C and I_B vs V_{BE} and h_{FE} vs I_B for a Typical Transistor Geometry (2)

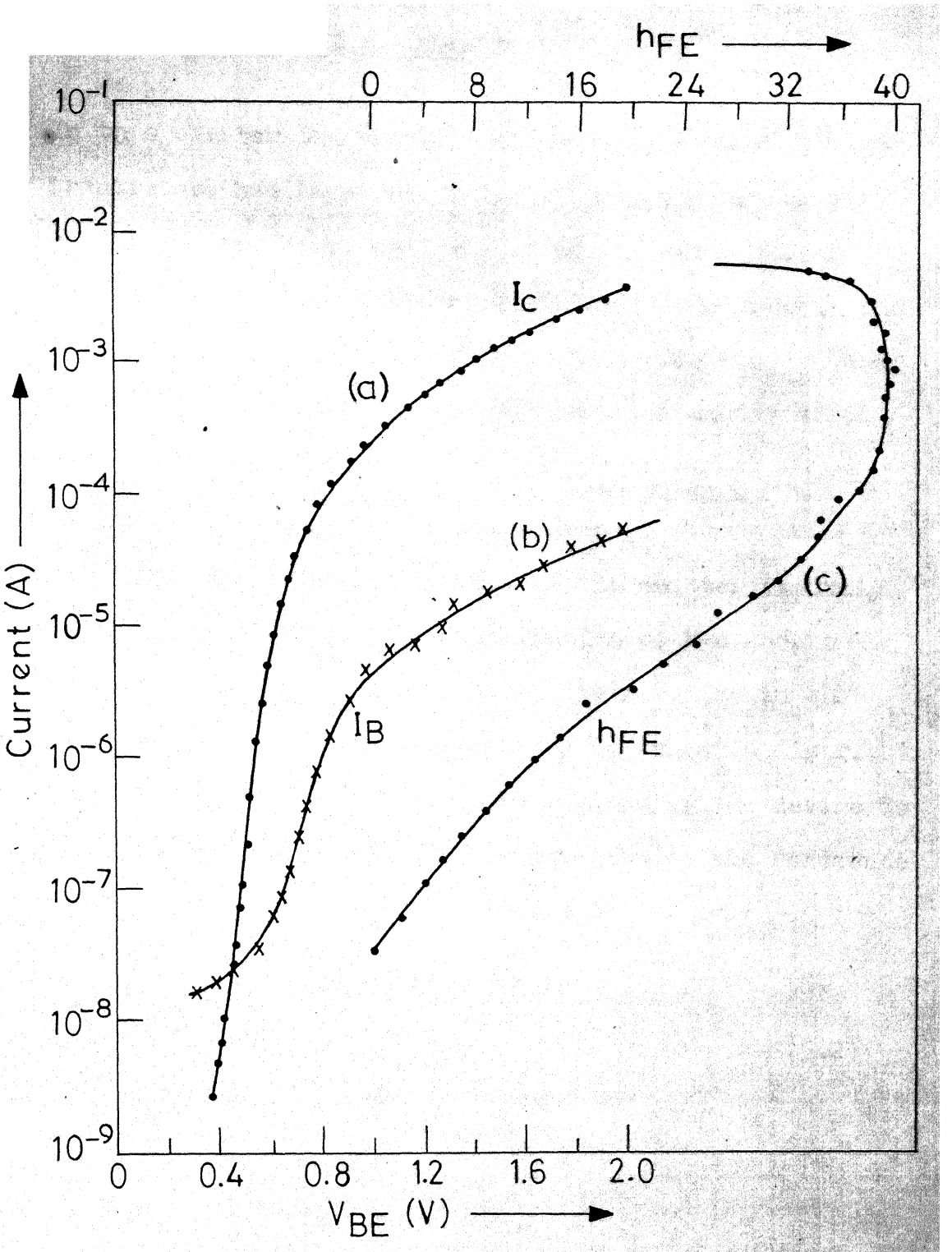


Fig.4.8 Plots of I_c and I_B vs V_{BE} and h_{FE} vs I_E for a typical transistor geometry (3).

CHAPTER 5

RESULTS AND DISCUSSION

In this chapter the common-emitter current-gain in high frequency transistors has been calculated using a simple model. The experimental and the calculated values of the current-gain have been compared to establish the credibility of the model. The dependence of the maximum common-emitter current gain $h_{FE_{max.}}$ and the current carrying capability on the horizontal geometry of the transistor has also been discussed.

5.1 Calculation of Common-Emitter Current Gain

In making theoretical calculations the emitter impurity profile is approximated as box type distribution with a dopant concentration of $4x10^{19}$ cm^{-3}. The impurity distribution in the base region under the emitter is approximated by gaussian distribution. The impurity doping profile in the various regions of the device is shown in Fig.4.1. Using the emitter-base junction as the reference point, this can be represented mathematically as follows:

$$N(x) = N_E = 4x10^{19}\ cm^{-3} \text{ for } -1.2\ \mu m < x < \qquad (5.1)$$

$$N(x) = N_{BE} \exp\left[-\beta\left(\frac{x}{x_j}\right)^2\right] - N_C \text{ for } x > 0 \qquad (5.2)$$

where, $N_{BE} = 3x10^{17}\ cm^{-3}$

$N_C = 6x10^{15}\ cm^{-3}$

and β is the profile parameter.

Equation (5.2) shows that the dopant concentration at the emitter-base junction is $(N_B - N_C) \simeq N_B$, whereas the actual concentration at the junction is zero and increases to its maximum value N_B as x increases. This region of increase being very small, the point of maximum doping density N_B in the base region is assumed to be shifted to the emitter-base junction (i.e. $x=0$). This assumption is made to simplify the calculations.

The profile and the structural parameters of the transistor, used in the calculations are tabulated in Table 5.1.

The minority-carrier life-times, τ_{pE} in the emitter region and τ_{nB} in the base region are taken from the earlier work of Chamberlain and Roulston [14] and are shown in Table 5.3. These values are assumed because the doping concentrations and the junction depths, which are the main parameters effecting the life-time, in the device under consideration are more or less the same as those considered in the above study. The minimum values of the life-times have been considered by taking $\tau_{pE} = \tau_{pO}$ and $\tau_{nB} = \tau_{nO}$.

The minority-carrier diffusion lengths in the emitter and the base regions are evaluated with the knowledge of these carrier life-times and estimating the effective diffusion constants $\bar{D}_{nB}$ and $\bar{D}_{pE}$ in the base and the emitter regions respectively. To determine the effective values of D_{nB} and D_{pE}, the carrier mobilities in the two regions were calculated using the modified

Caughey-Thomas relations [16].

$$\mu(N) = \frac{\mu_{max.} - \mu_{min.}}{1 + \frac{N}{N_{ref.}}} + \mu_{min.} \qquad (5.3)$$

The values of Caughey-Thomas parameters are given in Table 5.2. The respective carrier diffusion coefficients were evaluated from the mobility values. While evaluating $\bar{D}_{pE}$, the effect of high doping on Einstein's relation has been taken into account [17]. In the base region, diffusion constant D_{nB} is calculated at different points and the effective value of D_{nB} is evaluated using the relation:

$$\bar{D}_{nB} = \frac{1}{W_B} \int_0^{W_B} D_{nB}(x)\, dx \qquad (5.4)$$

This integral is evaluated numerically using the 5-point Gauss Quadrature formula [23]. The base-width was divided into 30 equal segments to obtain a maximum error of $\pm$ .1%. The calculated values of $\bar{D}_{nB}$ and $\bar{D}_{pE}$ and the corresponding minority carrier diffusion lengths are tabulated in Table 5.3.

The diffusion-length of the electrons in the base region as expected, has been found orders of magnitude higher than the base-width. Thus the bulk recombination in the base region can be neglected. The diffusion-length of holes in the emitter region is a fraction of the emitter-region width but is of the same order of magnitude. Hence the bulk recombination in the emitter

region has to be taken into account.

At high doping levels above 10^{17} cm^{-3} the intrinsic carrier concentration is increased due to bandgap narrowing, which increases the effective minority carrier concentration. This corresponds to the reduction in effective doping and consequently the reduction in Gummel Number. The effective values of intrinsic carrier concentration at high doping level in the emitter and the base regions are evaluated using the empirical relations [1].

$$n^2_{ie}(T) = n^2_{io}(T) \exp \frac{q\ V_{go}(N)}{kT} \quad \text{for } T > 250^{o}K \qquad (5.5)$$

and $$V_{go}(N) = V_1 [F + \sqrt{F^2+C}] \quad mV \qquad (5.6)$$

where, $F = \ln (\frac{N}{N_o})$.

$C = 0.5$.

$V_1 = 9.0$ mV.

N = impurity concentration in cm^{-3}.

$N_o = 10^{17}$ cm^{-3}

$qV_{go} = \Delta E_{go}$ = bandgap narrowing.

$n_{io}(T)$ is the intrinsic carrier concentration in the lightly doped semiconductor at absolute temperature T. For silicon the value of n_{io} is 1.5×10^{10} cm^{-3} at 300°K.

The effective minority-carrier concentration is evaluated from $\frac{n_{ie}^2}{N(x)}$. The effective Gummel Number and the effective doping concentration in the emitter-region were calculated using the above results.

The effective value of the Gummel Number in the base-region was calculated using the relation:

$$\bar{Q}_B = \int_0^{W_B} N_B(x)\, dx. \qquad (5.7)$$

The value of this integral was evaluated numerically using the 5-point Gauss quadrature formula [23]. The base-width was divided into 30 equal segments to get the maximum error of $\pm$ .1%.

The effective values of the Gummel Number and the doping concentrations in the emitter and the base regions are tabulated in Table 5.4.

The collector-current density is calculated using the relation :

$$J_n = \frac{q n_i^2 \bar{D}_{nB}}{\bar{Q}_B} \qquad (5.8)$$

The base-current density is calculated taking into account the bulk recombinations in the emitter-region and is given by the relation

$$J_p = \frac{q n_{ie}^2 \bar{D}_{pE}}{\bar{N}_E L_{pE}} \operatorname{Coth}\left(\frac{X_{JE}}{L_{pE}}\right) \qquad (5.9)$$

where, X_{JE} is the emitter-base junction depth.

The common-emitter current gain h_{FE} is evaluated as a ratio of the collector-current to base-current.

Using the simple model, the common-emitter current gain h_{FE} has been obtained as 76. This is in reasonably good agreement with the measured value of about 40. If the bandgap narrowing effect is not taken into account, the calculated value of h_{FE} has been

found to be orders of magnitude higher than the measured value. This concludes that the bandgap narrowing is the most dominant effect in the shallow-junction transistors.

5.2 Factors which Degrade the Common-Emitter Current Gain

The measured low value of h_{FE} in comparison to the calculated value may be attributed to a number of effects. Important among these are listed below in order of their importance.

1. Surface Leakage Current:

As observed in section 4.3, the values of reverse-bias (3 volts) emitter-base and base-collector junction currents for the typical device are .32 μA and .6 μA respectively. These currents are unusually high and contribute significantly to the base-current. This results in reduced value of measured h_{FE} as compared to its theoretical value, when these currents are neglected.

2. Life-Time Approximation:

The value of minority-carrier life-time particularly in the emitter region plays an important role (in the form L_{pE}) in the present model used for h_{FE} calculation. The carrier life-time depends on a number of parameters including doping density, surface conditions, crystal quality, process induced defects and injection level. Since its value has not been determined by measurements, any uncertainty in its value influences the h_{FE} calculations dominantly.

3. Doping Profile Approximation

During the evaluation of the emitter and the base region doping profiles, the bulk resistivity has been calculated using the relation (4.1), which involves the factor $\frac{d}{dx}[\log_{10} \rho_s(x$ The value of the differential was evaluated graphically by drawing the tangents at different points of the plot of $\log_{10}[\rho_s(x)]$ vs x. The value of the differential thus evaluated consists of calculatio error, which in turn makes the calculation of bulk-resistivity erroneous. Hence the evaluation of doping profile consists of calculation error. Moreover, the doping profile in the base region has been assumed to be gaussian distribution instead of taking the experimentally evaluated value at each point. This effects the calculated value of Q_B as used in equation (5.7) for the evaluation of the collector-current density.

The doping profile in the emitter region has been assumed box type, thus neglecting the rather slow decay of doping concentration in the vicinity of the emitter-base junction. Both these factors influence the calculation of h_{FE}.

4. Parasitic Effects

The base-spreading resistance has been found to be significantly high (≈ 1.5 K ohm) as calculated in the appendix. As the injection level increases, this (base-spreading resistance) plays an important role in limiting the emitter current. Moreover, the collector bulk-resistance is also found not to be insignificant which in turn reduces the collection efficiency of the transistor.

Both these effects which have been neglected in the calculation may cause a significant decrease in the current gain.

5. Recombination in the Emitter-Base Junction Depletion-Region.

Even at moderate injection level i.e. when the injection current starts dominating the surface leakage current, there may be significant recombinations in the emitter-base depletion-region. This gives rise to increased base current and hence reduces the current gain h_{FE}. The base current due to recombinations in the emitter-base depletion region has been neglected during the h_{FE} calculations.

6. Effect of direct injection from the emitter to the base through the lateral emitter-base diode has also been neglected.

5.3 Variation of h_{FE} with Injection Level

The initial rapid increase in the value of h_{FE} with injection level as shown in Fig.4.6(c) may be assigned mainly to the fact that at low injection levels the surface leakage-current dominates over the injection current. The trend continues till the injection-current reaches to about .52A/cm^2 corresponding to an emitter-current of about 10 μA. The plot of I_B vs V_{EB} in Fig.4.6(b) also supports this explanation. The emitter-base junction voltage V_{EB} corresponding to $I_E \simeq 10\ \mu A$ is about 600 mV as seen in Fig.4.6 (c). The base-current I_B is found to increase very slowly till V_{EB} reaches 600 mV, which justifies that I_B in this region is dominated by the surface leakage-current. As V_{EB}

is increased beyond 600 mV, I_B increases exponentially which confirms the dominance of the injection current over surface leakage-current for $V_{EB} > 600$ mV.

Further increase in h_{FE} with the injection level, which is rather slow may be attributed to the following:

Firstly, the bandgap narrowing effect starts weakening as the injection level is increased [1]. This gives rise to increased emitter efficiency and thus increase in h_{FE}.

Secondly, the S-R-H (Shockley-Read-Hall) recombination in the emitter region increases with the increase in injection level [2]. This results in the increase of minority-carrier life-time in the emitter region, which in turn increases the emitter efficiency and hence increases the value of h_{FE}.

A sharp fall in h_{FE} at high-injection level, when the emitter current desntiy increases beyond 5 mA/cm^2 in a typical transistor, is observed in Fig.4.6(c). This drop is due to the dominance of high-injection effects as base-stretching, larger depletion-layer recombinations, parasitic effects and the dominant current-crowding effect at high-injection levels.

The average majority-carrier concentration in the base region is about 5×10^{17} cm^{-3}. The injection level at which the injected minority-carrier concentration becomes comparable to the majority-carrier concentration (known as high injection level) is estimated using the relation

$$J_I = \frac{q\bar{D}_{nB}\, n_e(0)}{W_B} \qquad (5.10)$$

where, J_I = injected current-density.

$n_e(0)$= excess minority-carrier concentration.

The value of emitter-current density at which the high injection starts as calculated by the relation (5.10) has been found to be around $5\times10^4 A/cm^2$, which is orders of magnitude higher than the measured value of $520A/cm^2$. This premature occurrence of high injection effect can be attributed to the crowding of current at the periphery of emitter.

Moreover, the base-current corresponding to the emitter current at which high injection effects start dominating (Fig.4.6) is .5 mA. The base-spreading resistance is about 50 ohms (as calculated in appendix). This shows a voltage drop of 25 mV across the base region. This is nearly equal to the thermal voltage V_T at 300°K. Thus the emitter-crowding is the dominant high-injection effect in the typical device under study.

5.4 Dependence of Maximum Current-Gain and Current-Carrying Capability on the Horizontal Geometry

It is observed from Table 4.1 that the transistor maximum current gain $h_{FE,max.}$ increases with an increase in the emitter periphery to emitter area ratio. This is a general feature observed for all the fabricated units. As this ratio increases for a given emitter area, the emitter-base contact

periphery increases. This reduces the effect of emitter crowding, which is responsible for the observed increase in h_{FE}. Thus to increase the current-gain, the emitter periphery should be maximised for a given emitter area.

The transistor current-carrying capability increases with increase in emitter periphery to base area ratio as is evident from the results in Table 4.1. For a constant value of base area, as the emitter periphery is increased, the current-carrying capability also increases because of lessening of emitter crowding. Similarly when the base area is reduced for a given emitter periphery, the current-carrying capability can be increased by reducing the base area. This is because of the reduction in the base area causes a reduction in the base spreading resistance outside the shadow of emitter. This (reducing base area for a given emitter periphery) is more useful in integrated transistors where the collector contact is also taken from the same side as emitter and base contacts and whole of the base area is equally important. Thus to increase the current-carrying capability maximum emitter periphery should be embeded into minimum base area.

Table 5.1

Profile and Structural Parameters of the Transistor used in Calculations

N_E	N_{BE}	N_C	W_B	X_{JE}	X_{JC}	β
4×10^{19} cm^{-3}	3×10^{17} cm^{-3}	6×10^{15} cm^{-3}	$.3\times10^{-4}$ cm	1.2×10^{-4} cm	1.5×10^{-4} cm	3.2

Table 5.2

Caughey-Thomas Parameters

	$\mu_{max.}$ $cm^2\ sec^{-1}\ volt^{-1}$	$\mu_{min.}$ $cm^2\ sec^{-1}\ volt^{-1}$	α	$N_{ref.}$ cm^{-3}
Holes	495	47.7	0.76	6.3×10^{16}
Electrons	1360	92.0	0.91	1.3×10^{17}

Table 5.3

Minority Carrier Lifetimes and Computed Values of Effective Diffusion Constants and Diffusion Lengths

$\tau_{pE} = 5.3 \times 10^{-10}$ sec.

$\tau_{nB} = 3.2 \times 10^{-7}$ sec.

$\bar{D}_{pE} = 3.06$ cm^2 sec.$^{-1}$

$\bar{D}_{nB} = 20.6$ cm^2 sec.$^{-1}$

$L_{pE} = 0.4 \times 10^{-4}$ cm.

$L_{nB} = 25.7 \times 10^{-4}$ cm.

Table 5.4

Computed Values of Bandgap Narrowing, Effective Gummel Number and Effective Majority-Carrier Concentrations

Emitter Region:

Bandgap narrowing at N_E (4×10^{19} cm^{-3}) = 108.1 meV.

Effective Gummel Number $\bar{Q}_E$ = 7.2×10^{13} cm^{-2}

Majority-Carrier Effective Concentration $\bar{N}_E$ = 6×10^{17} cm^{-3}

Base Region:

Gummel Number Q_B = 2.8×10^{12} cm^{-2}

Band gap narrowing at N_{BE} (3×10^{17} cm^{-3}) = 21.6 meV.

Effective Gummel Number $\bar{Q}_B$ = 2.2×10^{12} cm^{-2}

Majority-Carrier Effective Concentration $\bar{N}_B$ = 7.3×10^{16} cm^{-3}

Neglecting Band-gap narrowing, the calculated value of h_{FE}, using relations (5.8) & (5.9) = 4050.

CONCLUSION

High frequency transistors with three different emitter geometeries have been considered and fabricated. The design of the horizontal geometery was based more on the possibility of its fabrication in the laboratory with available facilities than to achieve some predetermined performance.

The device has been fabricated on an epitaxially grown $n\text{-}n^{+}$ wafer using double-diffusion process.

The common-emitter current gain as calculated from the knowledge of the material and device parameters using a simple model is found to be orders of magnitude larger than its measured value. However, the inclusion of bandgap narrowing into current-gain calculations leads to its calculated value of 76. This is in reasonable agreement with the measured value of 40, in view of the uncertainity in the minority carrier life time and diffusion constant values. This clearly shows the effect of bandgap narrowing to be dominant in determining the current gain in shallow junction devices. The bandgap narrowing effect shall become negligible if the emitter-base junction depth is increased such that the diffusion length of carriers in the emitter region is orders of magnitude less than the emitter depth.

The study of variation of current-gain (h_{FE}) with injection level reveals that the initial rise in the value of h_{FE} is due to the dominance of injection current over the surface leakage current

APPENDIX

The fabricated transistor geometry (1) is analysed to calculate the values of different parasitic elements and the gain bandwidth frequency f_T.

The material and the device parameters have been taken up from Table 5.1.

area of the emitter region	=	1935.5×10^{-8} cm.^{2}
area of the base region	=	16774.2×10^{-8} cm.^{2}
emitter width	=	38.1×10^{-4} cm.
emitter length	=	50.8×10^{-4} cm.
average resistivity of the base region under emitter area	=	.7 ohm-cm.
average resistivity of the base region outside the shadow of emitter	=	.035 ohm-cm.
resistivity of the collector region	=	.65 ohm-cm.
ideality factor	=	1.098
drift field factor $n = \ln \frac{N_{BE}}{N_{BC}}$	=	3.9
phase factor $m = .22 + .098 \ln \frac{N_{BE}}{N_{BC}}$	=	.6
emitter current	=	5 mA
emitter-base junction forward-bias	=	1.2 volts
base-collector junction reverse-bias	=	5 volts
X_{db} (from relation 2.6)	=	1×10^{-4} cm.

Calculation of Parasitic elements:

Base-spreading resistance r'_b = $r'_{b1} + r'_{b2}$

the resistance (r'_{b1}) of the base area under the emitter region (from relation 2.9)= 1.5 K ohm

the resistance (r'_{b2}) of the base area outside the shadow of the emitter (from relation 2.10)= 49 ohm

total base spreading resistance = 1.55 K ohm

resistance of the emitter region r_e = $\frac{kT}{qI_E}$

= 5.3 ohm

resistance of the collector region r'_c = $\frac{L_S \rho_C}{A_E}$

= 18 ohm

emitter-base junction capacitance C_{TE} (from Lawrence-Warner curves) = 3.36 pf.

base-collector junction capacitance $C_{TC}=C_{CO}+C_{CI}$

C_{CI} (from Lawrence-Warner curves) = 0.0575 pf.

C_{CO} (from Lawrence-Warner curves) = 0.439 pf.

emitter-base junction time constant τ_e (from relation 2.3) = 17.8 psec.

base transit time τ_b (from relation 2.4) = 8.42 psec.

collector depletion layer transit time τ_d (from relation 2.5) = 8.75 psec.

collector R-C charging time τ_c (from relation 2.7) = 8.93 psec.

total time delay τ_{ec} = 43.9 psec.

gain bandwidth frequency f_T (from relation 2.1) = 2.25 GHz.

maximum frequency of operation f_{max} is given by the relation:

$$f_{max} = \sqrt{\frac{f_T}{8\pi r_b' C_{TC}}}$$

$$= 343 \text{ MHz.}$$

The relative magnitude of the saturation currents due to different mechanisms are given as:

1. The saturation current due to edge injected carriers is given by the relation:

$$I_{edge} \simeq q D_{nB} h X_{JE} N_{BE} \left[\sqrt{\left(\frac{qE_{BS}}{2kT}\right)^2 + \left(\frac{1}{L_{nB}}\right)^2} - \left(\frac{qE_{BS}}{2kT}\right) \right]$$

where, h is the emitter periphery

E_{BS} is the electric field in the base region where the emitter junction comes to the surface. For a graded junction

$$E_{BS} = \frac{kT}{q} x \frac{n}{X_J}$$

if, $E_{BS} \gg \frac{2kT}{qL_{nB}}$,

$$I_{edge} \quad \frac{qh X_{JE}^2}{\tau_{nB}} \quad \frac{1}{n} \quad N_{BE}$$

From the above relation edge saturation current = 2.93×10^{-20}A.

2. Saturation current due to surface recombination of edge injected minority carriers is given by

$$I_{SB} \simeq q \, S \, N_{BE} \left[\frac{qE_{BS}}{2kT} + \sqrt{\left(\frac{qE_{BS}}{2kT}\right)^2 + \left(\frac{1}{L_{nB}}\right)^2} \right]^{-1}$$

where, S is the surface recombination velocity.

taking $S = 10^3$ cm. sec^{-1}.

$$I_{SB} \simeq 7.8 \times 10^{-20} \text{ A.}$$

3. Saturation current due to injected carriers is calculated using the relation:

$$I = I_S \left[\exp \left(\frac{qV_{EB}}{\eta kT} \right) - 1 \right]$$

This gives the value of $I_S \simeq 5 \times 10^{-16}$ A.

It is evident from the above calculation that the injection saturation current is orders of magnitude higher than the saturation currents due to edge injected carriers and the surface recombination of edge injected minority carriers. Hence only injected carrier current play a dominant role in calculating the common-emitter current gain h_{FE}.

REFERENCES

1. J.W. Slotboom and H.C. De Graaff, "Measurement of Bandgap Narrowing in Si Bipolar Transistors," Solid State Electronics, Vol.19, pp.857-862, 1976.

2. Michael S. Adler et. al., "Limitations on Injection Efficiency in Power Devices," IEEE Trans. on Electron Devices, Vol.ED-23, No.8, pp.858-863, 1976.

3. "HBG Boron Nitride Diffusion Sources"- Literature supplied by Carborundum Company.

4. Ramon U. Martinelli and Evelyn Jetter, "The Effects of Emitter Impurity Concentration on the High-Current Gain of Silicon n-p-n Power Transistors," RCA Review, Vol.38, No.1, pp.60-75, 1977

5. Edgar T. Casterline and James A. Benajamin, "Trends in Microwave Power Transistors," Solid State Technology, Vol.18, No.4, pp.51-56, 1975.

6. H.F. Cooke, "Microwave Transistors: Theory and Design", Proc. IEEE, Vol.59, No.8, pp.1163-1181, 1971.

7. W.E. Beadle et al., "Design, Fabrication and Characterization of a Germanium Microwave Transistor," IEEE Trans. on Electron Devices, Vol.ED-16, No.1, pp.125-138, 1969.

8. K. Reindl, "Spun-on Arsenosilica Films as Sources for Shallow Arsenic Diffusions with High Surface Concentration," Solid State Electronics, Vol.16, pp.181-189, 1973.

9. D. Rupprecht and J. Stach, "Oxidized Boron Nitride Wafers as an In-Situ Boron Dopant for Silicon Diffusions," J. of the Electrochemical Society, Vol.120, No.9, pp.1266-1271, 1973.

10. K.R. Dunham, "Solid State Photoresist Technology," Solid State Technology, pp.41-47, June 1971.

11. Kenneth G. Clark, "Properties and Processes for Photoresists in Semiconductor Manufacture Pt.I," Solid State Technology, pp.52-56, June 1971.

12. Bruke Leon, "Photoresist Scumming, Pt.I. The Nature of Negative Photoresist Scumming," Solid State Technology, Vol.20, No.4, pp.71-77, 1977.

13. Literature on "Silica Film and Arsenosilica Film" supplied by Emulsitone Company, 41 East Willow St. Millburn, New Jersey 07041.

14. N.G. Chamberlain and D.J. Roulston, "Determination of Minority Carrier Lifetimes of Bipolar Transistors from Low-Current h_{FE} Fall-Off," IEEE Trans. on Electron Devices, pp.1346-1348, 1976.

15. Evans and Donovan, "Alternative Method for Converting Incremental Sheet Resistivity Measurements into Profiles of Impurity Concentration," Solid State Electronics, (Notes) Vol.10, pp.155-157, 1967.

16. D.M. Caughey and R.E. Thomas, "Carrier Mobilities in Silicon Emperically Related to Doping and Field," Proc. of the IEEE (Letters), Vol.55, No.12, pp.2192-2193, 1967.

17. F.A. Lindholm and R.W. Ayers, "Generalized Einstein Relation for Degnerate semiconductors," Proc. of the IEEE (Letters), Vol.56, No.3, pp.371-372, 1968.

18. W.R. Runyan, "Semiconductor Measurements and Instrumentation," McGraw-Hill Book Co., New York, 1975.

19. R.M. Burger and R.P. Donovan, "Fundamentals of Silicon Integrated Device Technology," Vol.I, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1968.

20. R.M. Burger and R.P. Donovan, "Fundamentals of Silicon Integrated Device Technology," Vol.II, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1968.

21. "Intensive Course on Semiconductor Device Technology," (December 4-14, 1974) Lecture Notes, Advanced Centre for Electronic Systems and Department of EE, IIT, Kanpur.

22. S.K. Ghandhi, "The Theory and Practice of Microelectronics" Mc-Graw-Hill Book Co., New York, 1963.

23. A. Ralston, "A First Course in Numerical Analysis," McGraw Hill Kogakusha Ltd., 1965.

24. A.S. Grove, "Physics and Technology of Semiconductor Devices," John Wiley and Sons, Inc., New York, 1967.

EE-1878-MT-GOX-DES